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INTEGRATION TECHNOLOGY OF FERROELECTRICS AND THE PERFORMANCE OF THE INTEGRATED FERROELECTRICS

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Abstract We have successfully incorporated the ferroelectric and the high dielectric constant capacitors into integrated circuits. The GaAs MMICs with BST capacitors have been widely used for cellular phones. The BST technology is also applied to a silicon CCD delayline processor for VCRs and camcorders. With respect to the ferroelectric technology with Y1, an experimentally fabricated 256k bit FeRAM has exhibited the remarkable performance of the 100 ns and 3V operation with a 1T/1C cell configuration dedicated for the FeRAM. These integrated ferroelectrics have been achieved by controlling the ferroelectric properties in thin films and incorporating the films into GaAs and silicon devices with outstanding process technology. Furthermore, we refer to the memory cell design technology which enables the FeRAM to work below 1V. Various advantages of low-voltage and high-speed operation inherent in integrated ferroelectrics will be emphasized on the intelligent microelectronics applications toward the next multimedia generation.

1. INTRODUCTION

A class of bismuth-layered oxide materials, Y1, has shown the innovative characteristics such as the fatigue free operation (> 1 x 10^{13} cycles), the very low imprint effect, and the

low coercive force, and therefore Y1 emerges out as an alternative to lead zirconate titanate (PZT) for nonvolatile memory applications.[1] In addition, barium-strontium titanate ($Ba_{1-x}Sr_xTiO_3$, commonly called BST), one of the high dielectric constant materials with the perovskite structure, has been proved of its promising features for dynamic random access memory (DRAM), GaAs microwave-monolithic integrated circuit (MMIC) and low electro-magnetic interference (EMI) LSI applications in terms of the high dielectric constant (> 300) at very thin film thicknesses and the low leakage current ($< 1 \times 10^{-8}$ A/cm^2) at required operating voltages in these devices.[2,3]

We have successfully incorporated the ferroelectric and the high dielectric capacitors into the integrated circuits. The GaAs MMICs with the BST capacitors have been widely used for cellular phones.[4,5] The technology is also applied to a silicon CCD delayline processor for VCRs and Camcorders.[6,7] With respect to the ferroelectric technology with Y1, an experimentally fabricated 256 kbit FeRAM has exhibited the remarkable performance of the 100ns and 3V operation with a 1-transistor and 1-capacitor per bit (1T/1C) cell configuration dedicated for the nonvolatile ferroelectric random access memory (FeRAM).[8]

In this paper, we will describe the technology for integrating the ferroelectric thin film capacitors into various functional devices, which meets the requests from the commercial applications. In addition, we will also demonstrate the superior performance of the FeRAM with state-of-the-art material and ferroelectric cell-design technology which enables the FeRAM operation below 1.0 V for the first demonstration to our best knowledge.[9]

2. INTEGRATION TECHNOLOGY

2.1 Preparation of Ferroelectric Thin Films

The metallo-organic decomposition (MOD) technique is preferable for growing ferroelectric thin films for low density device applications because of their simple device structure with a film thickness of typically 150 - 200 nm. Figure 1 shows a schematic flow of a typical MOD technique. Ferroelectric thin films are deposited on the substrate by spin-on coating of a homogeneous solution containing the stoichiometry correct precursors with subsequent drying and annealing for crystallization.[10] The spin-on technique allows low

machine overhead for manufacturing the integrated ferroelectric devices as well as stoichiometry correct films with the solution. A typical result of this technique using a BST solution is shown in Fig.2. The lattice constant of the BST thin films as a function of the Sr concentration is almost same as that of bulk ceramics. This result ensures that bulk ferroelectric properties can be obtained also in thin films.

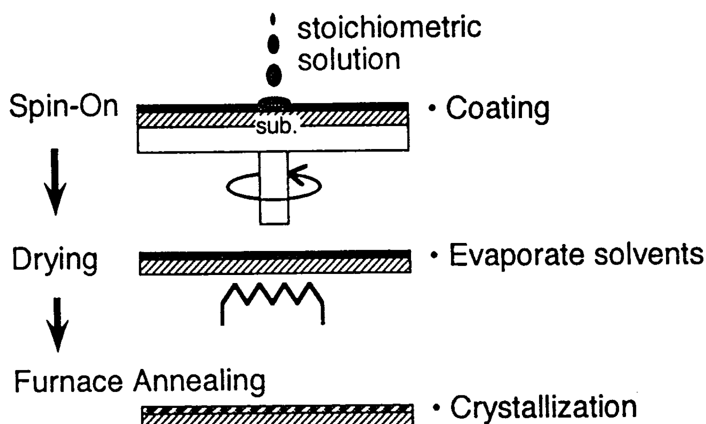


FIGURE 1 A schematic flow of metallo-organic decomposition (MOD) of a $Ba_{1-x}Sr_xTiO_3$ solution.

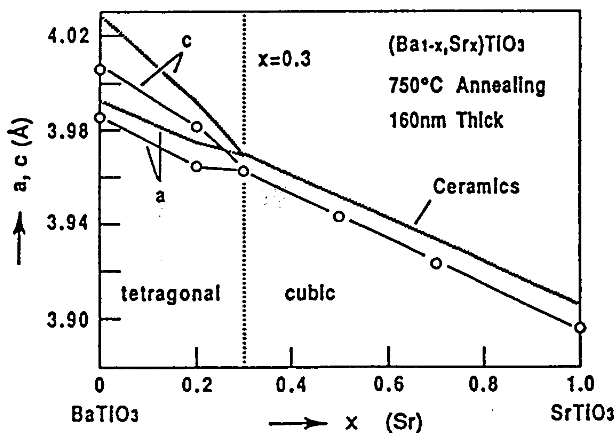


FIGURE 2 Lattice constants of bulk and thin film $Ba_{1-x}Sr_xTiO_3$ as a function of mol fraction of Sr.

Although the excellent composition controllability of the MOD spin-on technique, uniform films are obtained only on planar substrates and the thickness is limited down to 100 nm. For higher density devices with fine and complicated structures, such as multimegabit DRAMs and FeRAMs, the film thickness becomes smaller than 100 nm and then superior step-coverage is demanded. Taking the advantages of the MOD technique, a liquid source misted chemical deposition (LSMCD) technique using similar MOD liquid precursors was introduced.[11] A schematic diagram of the LSMCD machine is illustrated in Fig. 3. This technique is capable of unlimited choice in liquid precursor materials and no need for further composition control during the deposition at room temperature. Therefore this technique is also applicable for bismuth-layered ferroelectrics for high density FeRAMs as well as for high dielectric constant materials for gigabit-scale DRAMs.[12,13]

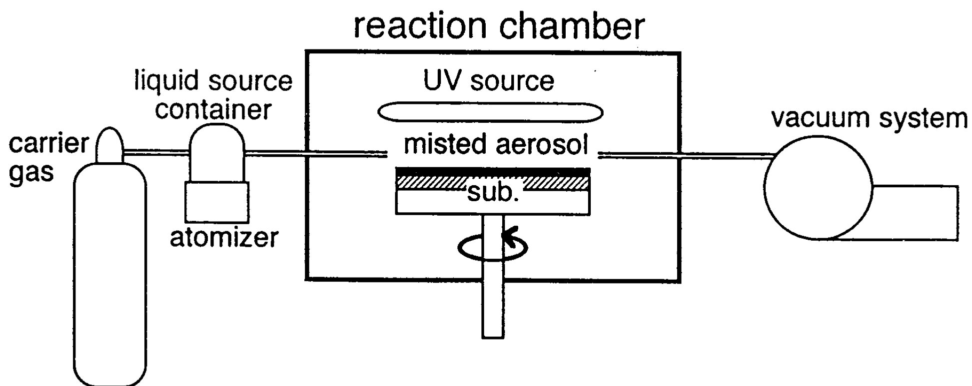


FIGURE 3 A schematic diagram of the LSMCD machine.

2.2 Patterning of Integrated Capacitors

Since ferroelectric materials of metal-oxide ferroelectrics and platinum for the electrode are chemically stable, there is a crucial issue to obtain fine patterns by chemical wet and/or dry etching. Although ion milling is one of the widely used patterning techniques, the high energy ion bombertment causes serious damage to underlaying MOS transistors and residual particles. In addition, uniform etching of capacitors with a fine structure on a wafer of more than 6 inches is difficult due to the poor etch selectivity to the underlaying materials.

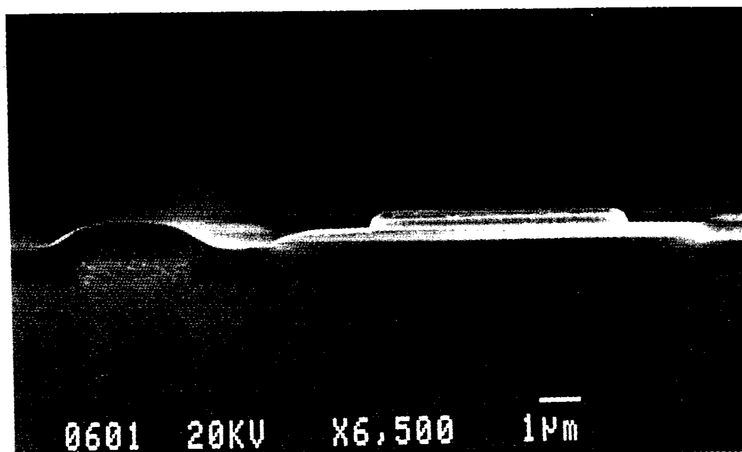


FIGURE 4 A cross sectional micrograph of a Pt/BST/Pt capacitor fabricated by reactive ion etching.

To obtain better ferroelectric/Pt and Pt/SiO_2 etch selectivities, we examined a variety of halide mixtures for magnetron reactive ion etching (RIE), and some of the mixtures were optimized for the materials to be etched. Figure 4 shows a cross sectional micrograph of a Pt/BST/Pt capacitor fabricated with a RIE machine, which demonstrates the highly selective RIE technology without undercutting of Pt bottom electrode and SiO_2 underlayer. Platinum and BST etch rates over SiO_2 are both from 50 to 100 nm/min with the high selectivities. With a proper choice of process gases and etching conditions, the RIE will challenge the sub-half micron lines and spaces required for megabit-scale DRAM fabrication.

3. ELECTRICAL PROPERTIES OF INTEGRATED FERROELECTRICS

3.1 High Dielectric Constant Material (BST)

Recent efforts toward the applications of spin-coated BST thin films to GaAs MMICs and bypass-capacitor-incorporated microcontrollers have proved of their potential opportunities for signal processing applications as well as memory applications.[3-7] The current-voltage characteristics of a $Ba_{0.7}Sr_{0.3}TiO_3$ film with a thickness of 140 nm prepared by the spin-on technique are shown in Fig. 5.[14] The leakage current in the BST film is 2×10^{-9} A/cm^2

at 3.3V, which is low enough to achieve the low power DRAMs.

Figure 6 shows the frequency dependence of the dielectric constant of BST. The dielectric constant is constant over the frequency range of more than 2 GHz.[3] This is due to the absence of ferroelectricity in BST thin films[15] as well as due to the paraelectricity at room temperature as shown in Fig. 2. Accordingly, integrated BST capacitors for high frequency applications are readily obtained.

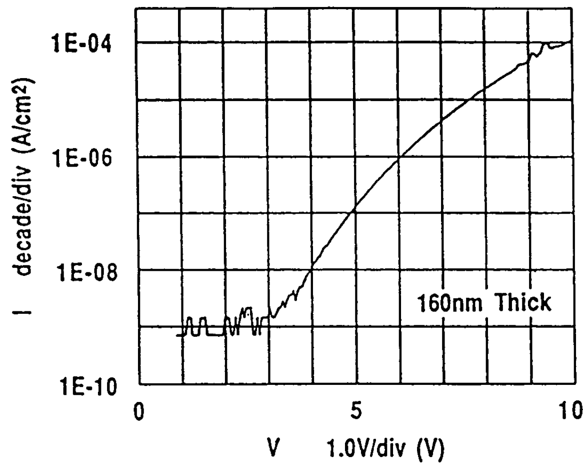


FIGURE 5 Current-voltage characteristics of a $Ba_{0.7}Sr_{0.3}TiO_3$ film with a thickness of 140 nm.

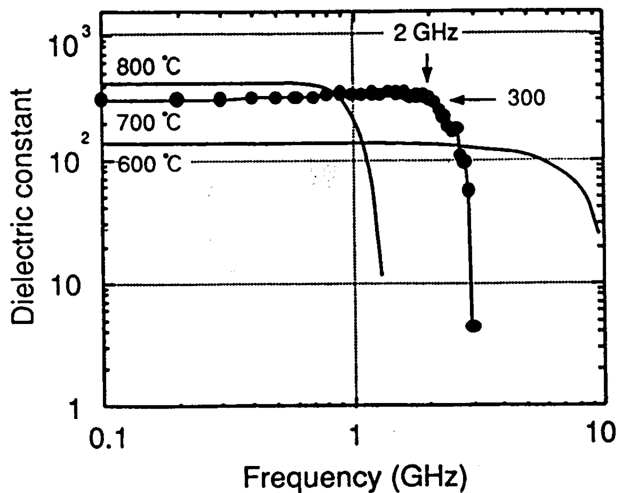
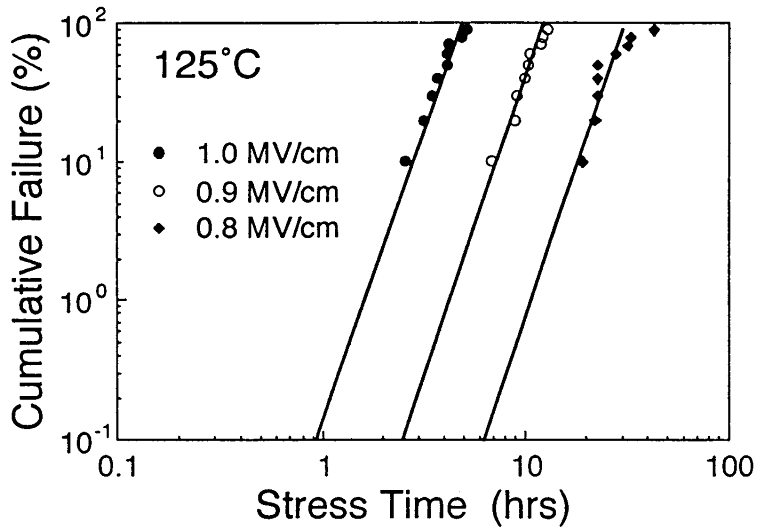
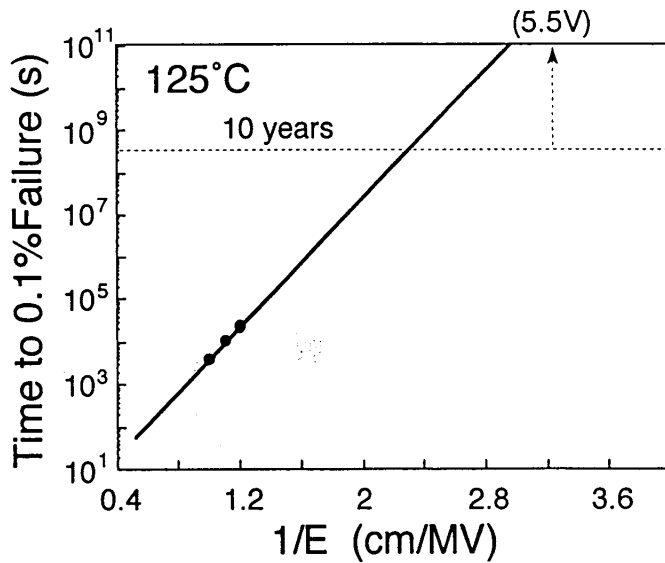


FIGURE 6 Frequency dispersion of the dielectric constant of $Ba_{0.7}Sr_{0.3}TiO_3$.



(a) Cumulative failure vs. stress time.



(b) Time to 0.1 % failure vs. reciprocal of field.

FIGURE 7 Time to failure dependent on the stress field for integrated BST capacitors with a thichness of 185 nm.

Figure 7 shows a Weibull plot for the cumulative failure in percent versus the stress time and thereby the 0.1 % cumulative failure as a function of reciprocal of the field for the integrated BST capacitors in a microcontroller. Since the structure factor *m* in Fig. 7(a) is greater than unity, the failure mode of the integrated BST films is intrinsic. From Fig. 7(b), an estimated life of with 0.1 % cumulative failures at 5.5 V is longer than 10 years, which ensures the reliable performance of the integrated BST capacitors.

3.2 Nonvolatile Material (Y1)

The remnant polarization decay in ferroelectric capacitors must be minimized for use in nonvolatile memory applications. This is characterized by fatigue after read/write cycles and becomes significant when PZT films are used in the memory capacitors. In PZT films, space charges at electrode interfaces are believed to be responsible for fatigue.[16,17] Although several advances in electrode materials, such as RuO_2, LaSrCoO, and IrO_2, have been reported to achieve read/write cycles of up to 10^{12} cycles without fatigue, the imprint effect in the hysteresis loop, which is characterized by the drift in the coercive field, still remains to be solved.[18]

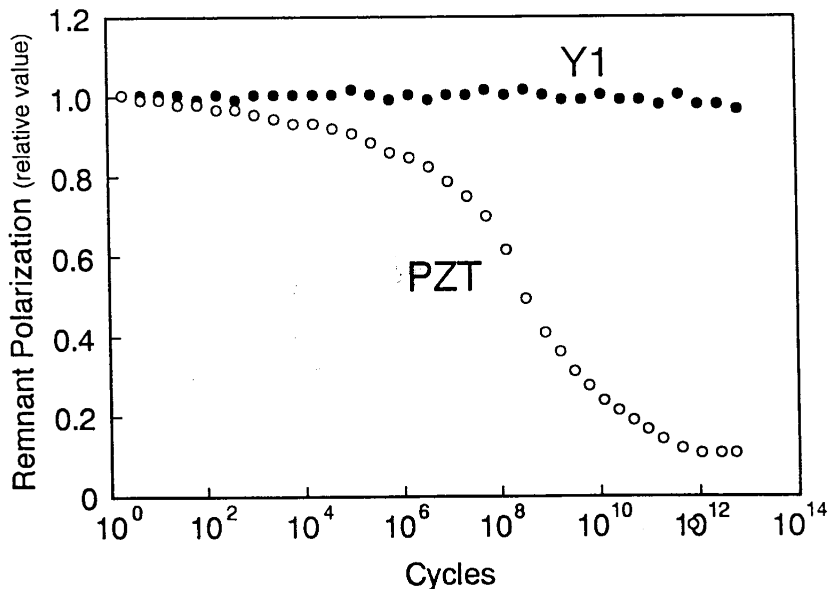


FIGURE 8 Endurances of Y1 and PZT after fatigue.

An out standing breakthrough in designing the materials for FeRAMs has been made by considering the atomic level microstructure of ferroelectrics.[1] In the bismuth-layered oxide material, Y1, the space charges probably due to oxygen vacancies can be compensated by the stacked oxide interlayers in itself. Therefore the bismuth-oxide material is hardly to degrade in remnant polarization or coercive field by the influence of electrodes. Figure 8 compares the endurance of remnant polarizations of ferroelectric capacitors with Y1 and with PZT after fatigue. A fatigue free read/write operation with Y1 is demonstrated up to 10^{12} cycles at 10MHz and 200 kV/cm. Figure 9 shows typical hysteresis loops of Y1 measured at low voltages of 0.9 and 1.5 V, where the remnant polarization is 8 μC/cm^2 and the coercive field is lower than 50 kV/cm. These results support the durability of Y1 in extremely low voltage operation nonvolatile memories.

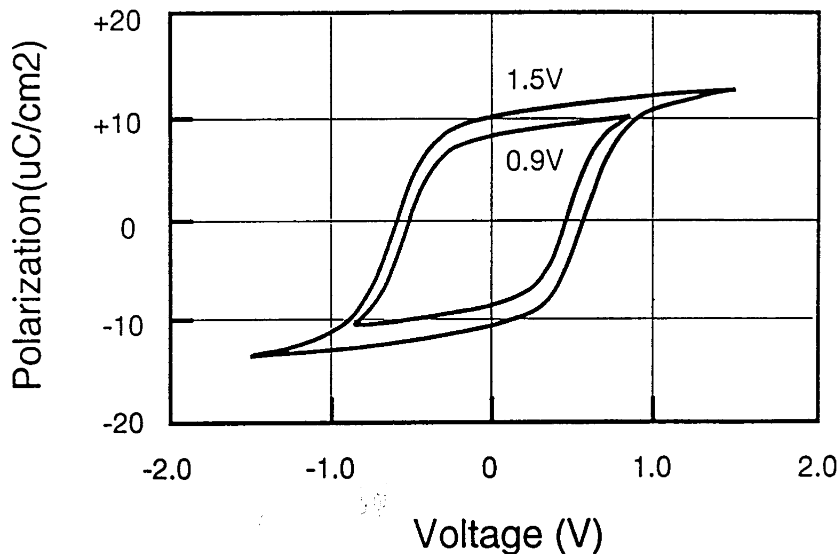


FIGURE 9 Typical hysteresis loop for a Y1 capacitor.

4. APPLICATION OF INTEGRATED FERROELECTRICS

4.1 Integrated BST Capacitors

By the use of BST, an integrated capacitor with a large capacitance of 100 pF/μm^2 can be formed in semiconductor devices without enlarging their chip size, which leads to the

reduction of the number of the lead pins for external bypass capacirors and the reduction of the parasitic inductance on the source and ground lines which results in lowering of EMI among high-speed analog/digital devices. The integration of the high dielectric constant capacitors has already been dedicated for commercial GaAs MMICs for mobile communications and silicon CCD delayline processors for VCRs and Camcorders. Figure 10 shows a photograph of the completed GaAs MMIC chip with a size of 0.55 x 0.9 mm^2. The integrated on-chip capacitors enable the implementation of the chip in a small 6-pin package.[4,5]

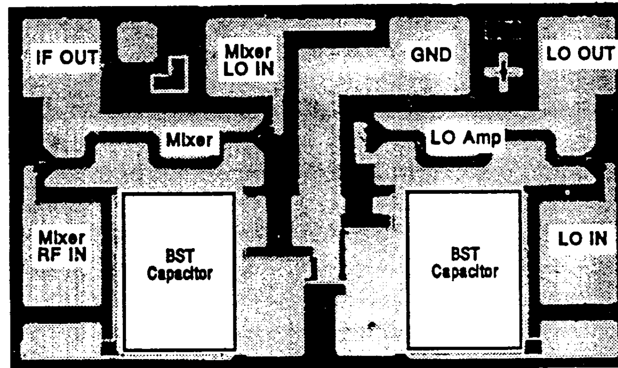


FIGURE 10 A photograph of a fabricated mixer IC for mobile communications.

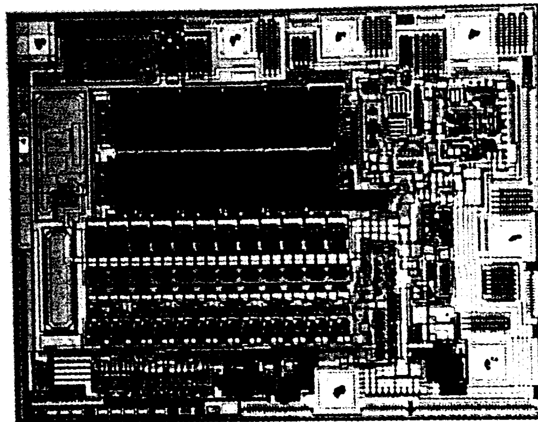


FIGURE 11 An analog/digital hybrid CCD delayline processor with a size of 1.8 x 2.3 mm^2.

Figure 11 shows an analog/digital hybrid CCD delayline processor with a size of 1.8 x 2.3 mm^2. A BST capacitor with a capacitance of 1400 pF is integrated in the left side of the chip. The footprint of the capacitor is 100 times smaller than that of the SiO_2 capacitor. The integrated BST capacitor is also effective enough to reduce undesirable noises on the source and ground lines by 70% in amplitude.[6,7] As a result, peak intensities in EMI spectra were reduced by 10 dB. Eventually this result promises that the application area of BST will be extended to signal processing devices.

4.2 DRAM Applications

In the manufacture of DRAMs larger than 16 Mbits, stacked cell structures are now displacing trench structures. To keep sufficient storage capacitance in the small memory cell area, complicated DRAM cell structures have been proposed to date by complicating their structures, such as fin or cylindrical shapes. Integrating the BST capacitor, however, sufficient capacitance is readily obtained in simple cell structures because of the high dielectric constant. For instance, 1-nm equivalent SiO_2 thickness is obtained for BST thin films with a thickness range of 50 - 150 nm. This equivalent SiO_2 thickness is a quarter of the minimum dielectric thickness limited by tunneling current in SiO_2.

Figure 12 illustrates a DRAM cell structure using the BST thin film in the storage capacitor with a Pt/TiN/Ti interface to the storage node. The Pt/TiN/Ti interface intercepts

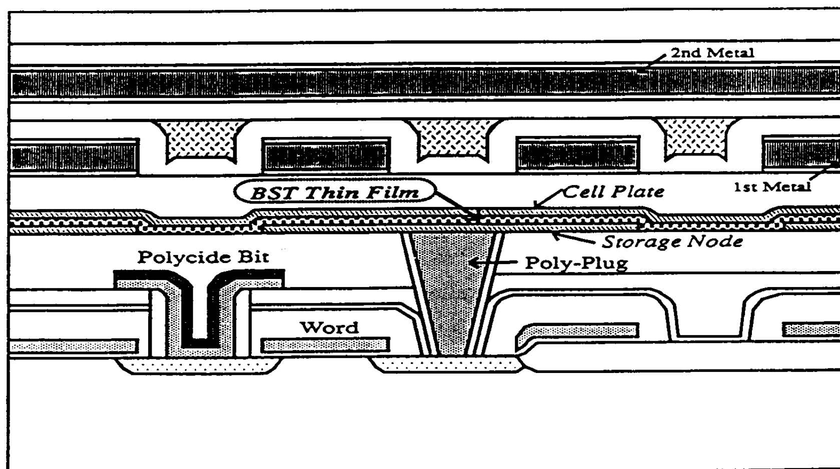


FIGURE 12 A DRAM cell structure using BST in the cell capacitor.

the diffusion of Si in the plug to BST.[2] This simple cell structure proves that the stacked cell structure currently employed in 4 or 16 Mbit DRAMs is still applicable to 256 Mbit or 1 Gbit DRAMs by virtue of integrating the BST thin films. This planar-type single stacked cell was achieved not only by the newly developed storage node structure but also by the advanced RIE technology.

4.3 Fatigue Free FeRAMs

One of the prominent characteristics of FeRAMs using Y1 is the fast read/write operation at low voltages, because switching of dipoles in Y1 from one polarization state to another is completed in several tens nanoseconds.[1] This technology has been established in a 1T1C cell configuration currently used in DRAMs, which allows higher density integration of memory cells. Figure 13 shows a photograph of an experimentally fabricated 256 kbit FeRAM chip featuring the 1T1C cell structure using Y1. The memory cell effectively operates at 3V with a read/write cycle of 100ns.

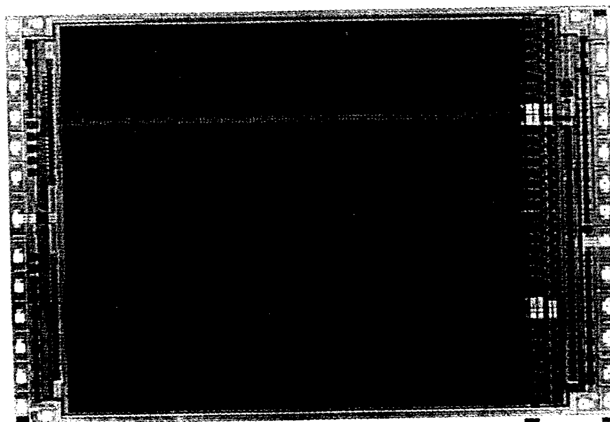


FIGURE 13 An experimentally fabricated 256 kbit FeRAM incorporating ferroelectric capacitors using Y1. The chip size is 5.3 x 7.9 mm^2 and the memory cell size is 11.4 x 7.5 μm^2.

Another important factor in designing the FeRAM is a need for reference voltage to discriminate whether the read-out data is in high or low logic level. To achieve an enhancement of the read-out voltage over the wide range of the source voltage, a preset

reference cell was introduced.[8] Figure 14 shows the preset reference circuit used in the 256 kbit FeRAM. In a conventional reference cell configuration without the preset transistors in the circles in Fig. 14, the voltage across the reference capacitor is unstable because the voltage depends on the preceding read-out data on the memory cell. When the voltage on the reference word line (RWL) and the cell plate (CP) go low levels preparing for the next read-out cycle, the voltage at floating node A becomes zero or the level of built-in voltage at the p-n junction . Addition of the preset reference circuit with the preset transistors ensures the voltage across the reference capacitor is zero independent of the read-out data, which gives a wide margin for low voltage operation.

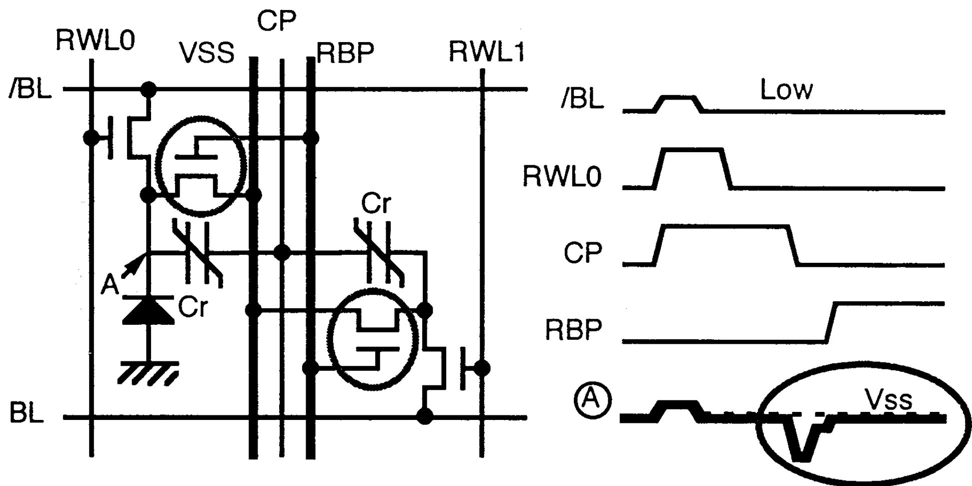


FIGURE 14 Preset reference circuit designed for a 256 kbit FeRAM.

The third important factor is how a layered metal oxide model containing materials design, process sensitivity, and device physics can be used in the design of FeRAMs. Figure 15 shows the read-out voltage on a bit line pair as a function of ratio of parasitic bit line capacitance to ferroelectric cell capacitance (C_{BL}/C_S). If a linear capacitance model is invoked, a large read-out voltage in the small C_{BL}/C_S region is estimated. Simulation using a physically accurate device model, on the other hand, shows good agreements with measurements and is therefore essential for low-voltage and high-speed FeRAM design.[9]

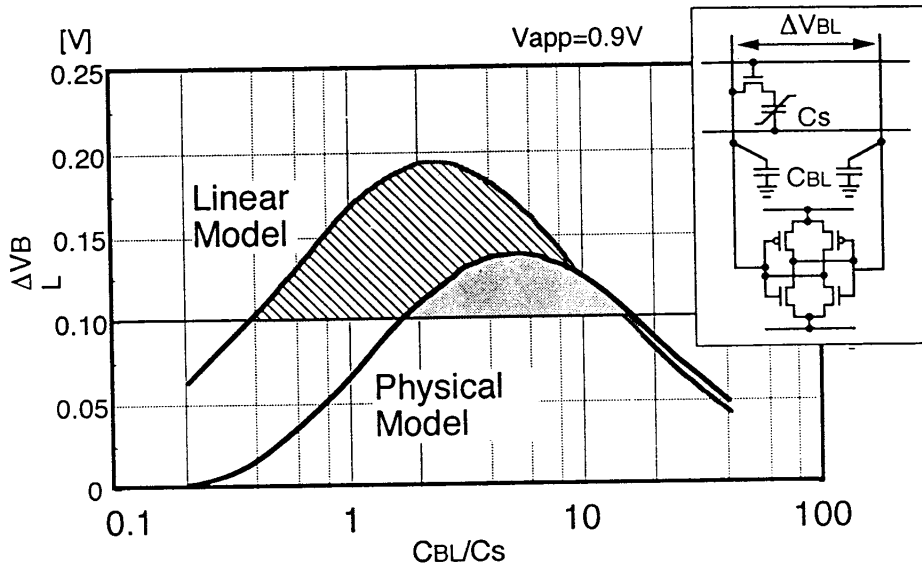


FIGURE 15 Read-out voltage on a bit line pair as a function of ratio of parasitic bit line capacitance to ferroelectric cell capacitance (C_{BL}/C_S).

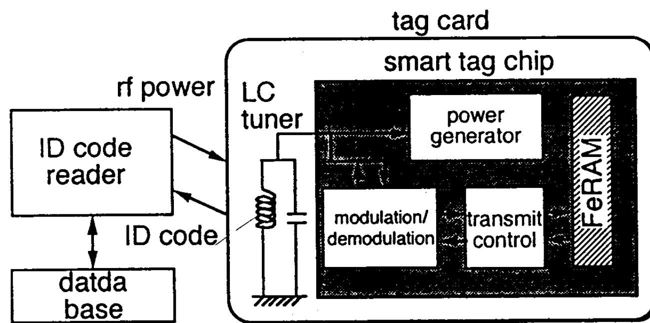


FIGURE 16 RF-ID tag system.

Another application of low-voltage and high-speed nonvolatile memories using Y1 is intended to RF-IDs (Fig.16). Since the operation power is supplied by transmitting rf power of itself, an RF-ID with an embedded FeRAM must operate at low voltages in far remote access distance. In addition, high-speed operation is needed to complete read/write cycles in short time for mobile applications. The high-speed read/write operation of the

FeRAM then promises real-time update of stored programs as well as stored data in the FeRAMs.

Not only FeRAMs are nonvolatile but also the high-speed operation is an enabling technology for enormous applications because the FeRAM has a ROM like function as well as a RAM like function. For instance, a microcontroller incorporating an EEPROM could be replaced by the FeRAM, where no discrimination between ROM and RAM is necessary.[9] Use of the FeRAM then becomes more flexible in particular in allocating memory area to program memory, data memory, and working sub-area, according to the application program as shown in Fig.17. In the not too distant future, memory functions in a microcontroller shared with an EEPROM and a SRAM will depend on a single on-chip FeRAM.

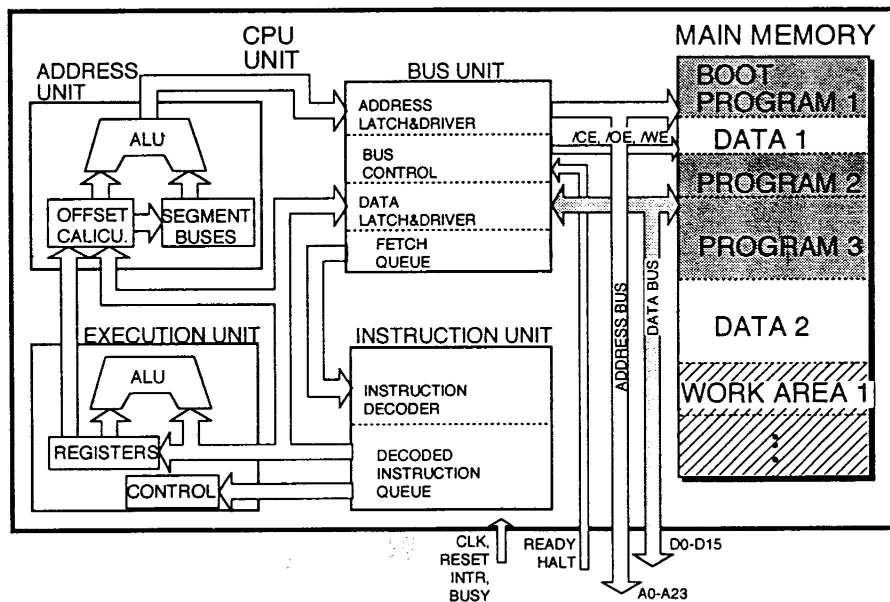


FIGURE 17 A FeRAM embedded microcontroller.

5. SUMMARY

Since several less-common materials, such as ferroelectrics and Pt, are used in integrated ferroelectrics, conventional silicon processing may not be applied directly to the ferroelectric integration process. The most advanced fabrication process for integrating ferroelectrics is limited to 1 μm in lines and spaces, while the silicon process is now going

under the sub-half micron range. One of these limitations arises from the difficulty in etching of ferroelectrics and the electrodes. Another is due to incompatibility with conventional silicon processes. Research now underway promises to address some of these limitations. [19]

To make the most of the integrated ferroelectrics, proper choice of ferroelectric materials should be made according to the device applications. For high density and large capacitance applications, processing of high dielectric constant materials such as BST is still evolving toward down sizing and simplification of conventional DRAM cell configurations. For nonvolatile memory applications, on the other hand, bismuth-layered oxide materials such as Y1 exhibit various advantages in fatigue-free, low-voltage, and high-speed update operations. In addition, use of the embedded FeRAM will boom across the microcontroller application field because of its flexibility in allocating the memory area.

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