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Temperature-Dependent Current-Voltage Characteristics of Fully Processed $Ba_{0.7}Sr_{0.3}TiO_3$ Capacitors Integrated in a Silicon Device

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Temperature-dependent current-voltage characteristics of fully processed $Ba_{0.7}Sr_{0.3}TiO_3$ thin film capacitors integrated in a charge-coupled device delay-line processor as bypass capacitors were studied. The thin film capacitors with a film thickness of 185 nm were formed by metal-organic decomposition processing. The leakage current measured after completion of the integration process was 1 to 2 orders of magnitude higher than that measured after capacitor patterning. The leakage current at low voltages (<1 V, 50 kV/cm) indicated ohmic conduction within a measured temperature range of 300–423 K. At high voltages (>10 V, 500 kV/cm), the Schottky mechanism plays a dominant role in leakage current, while the Frenkel-Poole emission begins to contribute to the leakage current as the temperature is elevated.

KEYWORDS: ferroelectrics, ferroelectric capacitor, BST, conduction mechanism

1. Introduction

Ferroelectric materials, particularly $Ba_xSr_{1-x}TiO_3$ (BST), $PbTiO_3$, and $Pb_xZr_{1-x}TiO_3$, have emerged as high-dielectric-constant capacitor materials for high-density integrated circuit (IC) applications, such as dynamic random access memory (DRAM) cell capacitors.[1] When they are incorporated into ICs, leakage current in these capacitors is one of the most important parameters for estimating the capacitor charge retention. Although a variety of data for the electrical properties of ferroelectric films with preliminary metal-insulator-metal (MIM) structures have been reported,[2–7] there are very few data concerning the electrical properties of fully processed integrated capacitors. One of the major reasons is the increase in leakage current by going through the capacitor integration processes on a substrate with metal-oxide-silicon (MOS) transistor ICs. For instance, thermal treatments in forming gases needed to stabilize the MOS transistors sometimes cause serious damage to the ferroelectric capacitors. Therefore, to obtain a better understanding of the electrical behaviors of ferroelectric capacitors in actual MOS devices, it is very important to characterize the electrical properties of fully passivated ferroelectric capacitors on a MOS device.

In this paper, we first report the current-voltage (J-V) characteristics of fully processed integrated $Ba_{0.7}Sr_{0.3}TiO_3$ capacitors incorporated in a charge-coupled device (CCD) delay-line processor and extract the possible current transport mechanisms in the integrated BST capacitors from the temperature dependence of the J-V characteristics.

2. Experimental

Among various ferroelectric materials, $Ba_{0.7}Sr_{0.3}TiO_3$ is one of the appropriate choices for realizing a high-dielectric-constant integrated capacitor because its stoichiometry is chosen to maximize the dielectric constant at the phase transition boundary.[2] In the present experiments, BST films were prepared by a metal-organic decomposition technique on Pt-deposited silicon wafers in which digital/analog filtering ICs are fabricated.[8,9]

A metal-alkoxide solution including 6 wt% BST was coated on the 300-nm-thick Pt-deposited wafers to obtain about 185-nm-thick crystallized BST films. After high-temperature annealing of the coated films in oxygen, Pt electrodes of 150 nm were deposited on the crystallized BST to form a MIM structure and a number of photomasked capacitors with the size of $200 \times 200\,\mu m^2$ were patterned using a plasma etcher. Subsequently, the capacitors were covered with interlayer silicon dioxide films formed by chemical vapor deposition and the interlayer films were etched using a plasma to form contact openings used to interconnect the capacitors and underlaying peripheral transistor circuits. After metallization with sputtered aluminum, interconnect patterns were formed by wet chemical processing. After post-metallization annealing in forming gas, silicon nitride films for passivation were deposited by plasma chemical vapor deposition and then bonding pad openings were formed by dry etching.

The J-V characteristics of the fully processed capacitors integrated in the silicon device were measured with a HP4145B semiconductor parameter analyzer at different temperatures in the range of 300–423 K. The capacitance-voltage (C-V) characteristics were measured with a HP4194A impedance/gain-phase analyzer. Optical constants of the BST films were measured with a Nano-Spec model 4000 microspectrometer.

3. Results and Discussions

Figure 1 shows typical J-V curves of a BST capacitor after the patterning of the MIM-structured capacitor and after completion of the integration process. The leakage current at an applied voltage of 3 V of the fully processed capacitor was increased from 10^{-8} A/cm^2 to 10^{-6} A/cm^2 due to the processing after the capacitor patterning. This increase in leakage current is ascribed to the degradation in resistivity of the BST films due to damage occurring during sputtering of metals, etching of contact holes, deposition of dielectrics or passivations, forming of underlaying transistors, or annealing of wafers. Even

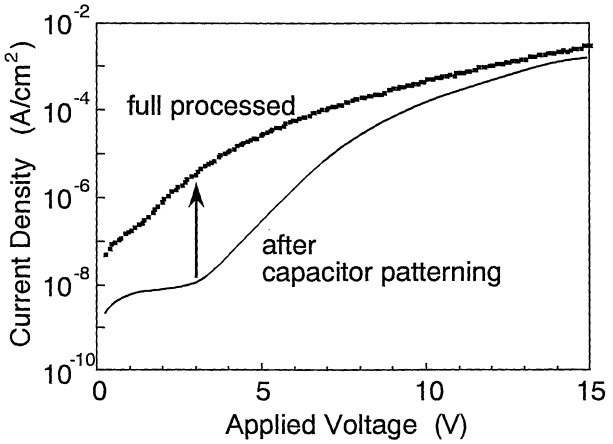

Fig. 1. Semilogarithmic plot of conduction current versus applied voltage for a typical integrated BST capacitor with size of $200 \times 200\ \mu m^2$ and thickness of 185 nm. The lower curve is for the capacitor after patterning. The upper curve is for the fully processed capacitor.

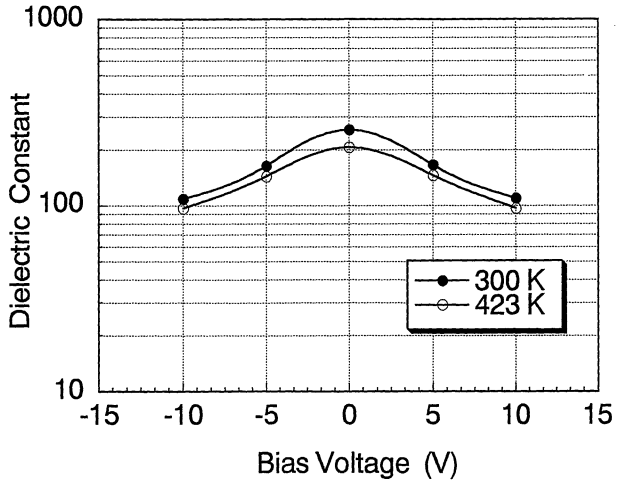

Fig. 3. *C-V* characteristics of integrated BST capacitors measured at room temperature under ac amplitude of ±0.5 V at 1 MHz.

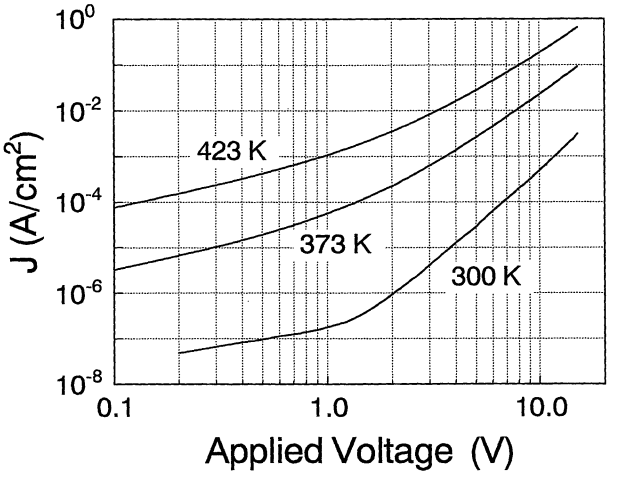

Fig. 2. Log-log plot of *J-V* data in Fig. 1, showing ohmic region below 1 V and different conduction behavior above 2 V.

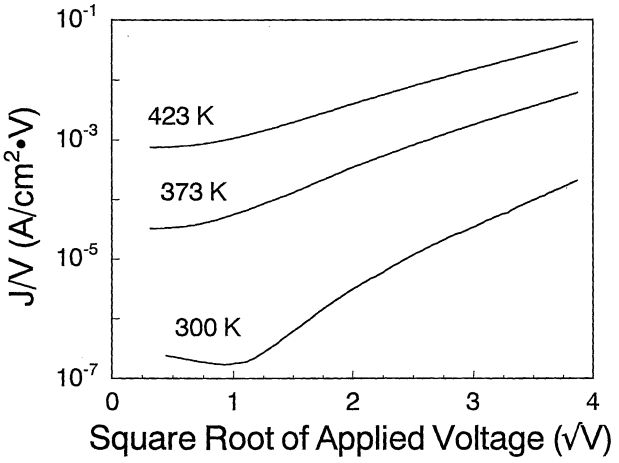

Fig. 4. The $\log(J/V)$–$V^{1/2}$ plot showing the Frenkel-Poole conduction relationships at high voltages.

with the increase in leakage current, the fully processed capacitor is of sufficient quality for use in MOS devices as a bypass capacitor because the leakage current level is much smaller than the stand-by current, typically on the order of milliamperes, of these devices. The integrated BST capacitors were then electrically tested for the leakage current in the temperature range from 300 to 423 K.

The *J-V* characteristics measured for the fully processed integrated BST capacitors at temperatures of 300, 373, and 423 K are shown in Fig. 2. Since we did not observe any asymmetry in the *J-V* behavior upon reversal of the polarity of applied voltage and obtained symmetric *C-V* curves as shown in Fig. 3, we will hereafter study the situation in which the top electrode is positively biased and consider bulk-controlled and symmetric-interface-controlled conduction mechanisms.[10–12] In Fig. 2, the leakage current is increased by several orders of magnitude as the temperature is elevated and the curves can be separated into two distinct regions according to the slope of the curves. At low voltages below 1 V (50 kV/cm) the curves show a linear dependence within the measured temperature range and each curve has a slope of approximately 1; this voltage dependence indicates an ohmic behavior. The curve measured at room temperature is followed by another linear region at high voltages (>2 V, 100 kV/cm) with a slope of more than 2. As the temperature is elevated, curves begin to deviate from the linear dependence due to the contribution of other conduction mechanisms to the total current.

The current transport in ferroelectric films at high fields is usually ascribed to Frenkel-Poole and/or Schottky emission mechanisms.[5,10–15] If the current transport at high voltages is governed by either one of these two mechanisms, the *J-V* characteristics at high voltages should have a linear dependence on the square root of applied voltage and the slope of a curve in the linear region should give the high-frequency dielectric constant ε.[14,15] To reveal these two mechanisms more clearly, the curves in Fig. 2 are replotted in Fig. 4 for the Frenkel-Poole mechanism and in Fig. 5 for the Schottky mechanism. The slope of the curves at high voltage for the Frenkel-

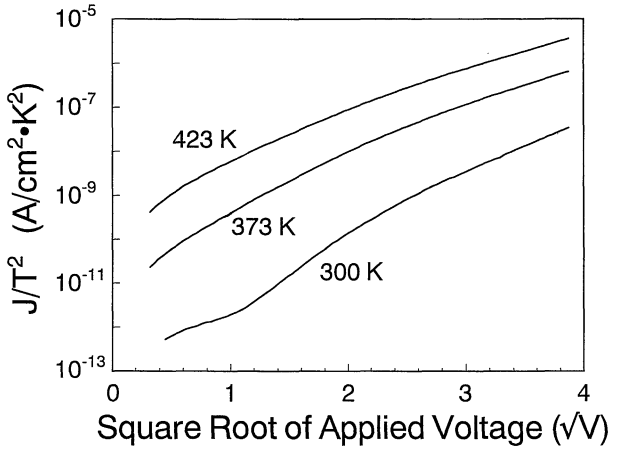

Fig. 5. The $\log(J/T^2)$–$V^{1/2}$ plot showing the Schottky relationships at high voltages.

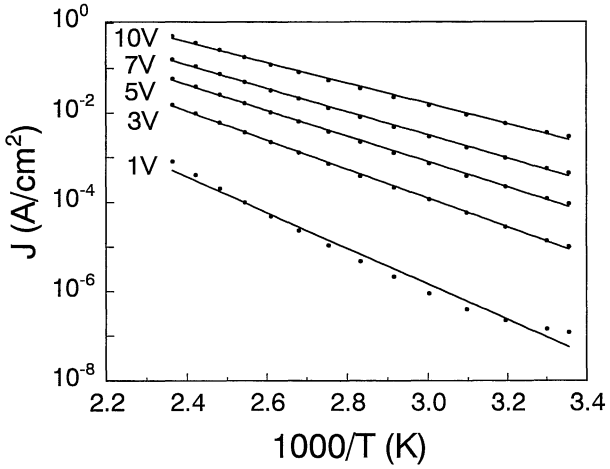

Fig. 6. Temperature dependence of current density of integrated BST capacitors for various applied voltages.

Poole mechanism yields $\varepsilon = 6.8$, 7.7, and 7.3, while for the Schottky mechanism the slope yields $\varepsilon = 2.8$, 3.9, and 4.1 at temperatures of 300, 373, and 423 K, respectively.

The dielectric constant of the BST film on Pt substrate was determined from an optically measured refractive index. Since $n = 2.0$ at 640 nm in wavelength and $\varepsilon = n^2$, where n is the refractive index, the high-frequency dielectric constant is then calculated to be 4.0. This value is closer to that of the Schottky mechanism than to that of the Frenkel-Poole mechanism. At high voltages and high temperatures, however, the linear region in Fig. 4 is wider than that in Fig. 5. In addition, the linear region in Fig. 4 is enlarged and the onset voltage of the linear region is lowered as the temperature is elevated. These results indicate that the contribution of Frenkel-Poole emission to the leakage current emerges as the temperature is elevated in the high voltage region. The electrical conduction in the integrated BST capacitor at high voltages is therefore substantially dominated by symmetric Schottky interfaces within the measured temperature region and bulk-controlled Frenkel-Poole emission begins to be superposed on the total current at high temperatures.

Figure 6 shows the activation energy plots of the current in the integrated BST capacitors at various applied voltages from 1 to 10 V. The current density increases by as much as three orders of magnitude within the measured temperature range. The activation energy, plotted in Fig. 7, decreases with the square root of applied voltage and shows good linearity at high voltages. An extrapolation of the curve at high voltages gives a barrier height of 0.8 eV. The linear dependence in the high voltage region is consistent with both the Frenkel-Poole and Schottky conduction mechanisms.

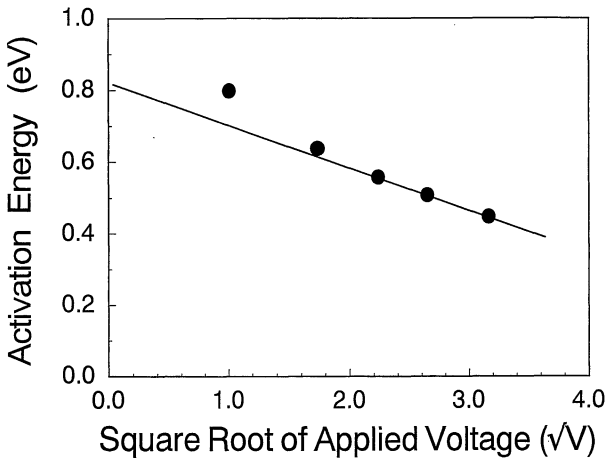

Fig. 7. Activation energy as a function of the square root of applied voltage.

4. Conclusions

Leakage current behavior of a fully processed BST capacitor formed on a MOS device was demonstrated. The leakage current measured at 3 V was increased from 10^{-8} A/cm^2 to 10^{-6} A/cm^2 as a result of the integration processed after the capacitor patterning. This increase in leakage current is assumed to be caused by degradation in resistivity of the BST film due to damage occurring during integration processing. The leakage current of the fully processed capacitor, however, is small enough to allow its practical use in MOS devices as a bypass capacitor. For further understanding of integrated ferroelectric capacitors, we studied the temperature dependence of J-V characteristics of the fully processed integrated BST capacitors. The current transport at low voltages (<1 V) is attributed to the ohmic conduction. At high voltages (>10 V), the Schottky mechanism is assumed to predominate, while the Frenkel-Poole mechanism begins to contribute to the leakage current as the temperature is elevated.

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