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Retention Characteristics of a Ferroelectric Memory Based on $SrBi_2(Ta, Nb)_2O_9$

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The polarization decay process in $SrBi_2(Ta, Nb)_2O_9$ capacitors and retention characteristics of a 288-bit ferroelectric memory device fabricated from $SrBi_2(Ta, Nb)_2O_9$ were studied. The remanent polarization decay at room temperature showed good linearity when plotted against logarithmic retention time over a wide range of 10^{-3}–10^5 s. The distribution of times to failure of a 288-bit memory was fit to a model having a linear relationship between $\log(\log t_f)$ and $1/T$ for the period of infant failures and to the Arrhenius model having the form $\log t_f$ vs $1/T$ for the period of random failures, where t_f is the time to failure and T is the temperature. The activation energy was found to be 0.35 eV for infant failures and 1.15 eV for random failures. Possible causes for the difference in activation energies are discussed.

KEYWORDS: ferroelectric memory, retention, bismuth-layered perovskite, $SrBi_2(Ta, Nb)_2O_9$

1. Introduction

Ferroelectric memory devices based on bismuth-layered perovskites such as $SrBi_2Ta_2O_9$ (SBT) and $SrBi_2(Ta, Nb)_2O_9$ (SBTN) have become an important class of nonvolatile ferroelectric memories because of their fatigue-free nature, exceeding 1×10^{12} read/write cycles.[1–4] For nonvolatile memory applications, however, the data retention performance is of reliability concern. The typical requirement for nonvolatile memories is that the data integrity must be guaranteed for more than 10 years over a wide range of temperatures, from −10 to 70°C for consumer applications and between −40 and 85°C for industrial applications.

The nonvolatility in ferroelectric memories is achieved essentially by preserving a sufficient amount of charge, which couples with the remanent polarization, in a storage capacitor to yield a voltage signal on a bitline greater than the marginal signal for a sense amplifier when a read voltage pulse is applied. However, the remanent polarization in ferroelectric capacitors using materials such as $Pb(Zr, Ti)O_3$ tends to decrease with not only increasing the temperature but also time.[5–8] Therefore, the long-term stability of remanent polarization and the temperature effects on the data retention performance are of much interest in ferroelectric memory applications.

In this paper, we report the polarization decay process in integrated SBTN capacitors and the temperature dependence of memory retention failures in an SBTN-based 288-bit ferroelectric memory device. From statistical results of the temperature-accelerated retention testing, possible failure mechanisms are discussed by introducing empirical reliability models which explain well the data retention characteristics of SBTN memories over a wide range of time.

2. Experimental

2.1 Sample fabrication

For the present experiment, we designed an SBTN capacitor array containing 110 elements and a 288-bit serial memory that incorporates SBTN cell capacitors. The capacitor size is $5 \times 5\,\mathrm{cm}^2$. Each memory cell is comprised of two transistors and two capacitors ($2T/2C$) with a cell size of $182\,\mu\mathrm{m}^2$. The 288-bit memory is organized into 18 rows by 16 bits. A typical access time of the memory is 230 ns at 5 V and room temperature. The SBTN capacitor arrays and 288 memory cells with Pt electrodes were fabricated using a spin-on technique on silicon wafers with an underlying peripheral drive circuit.[9] The capacitor arrays and memories were cut into dies, and assembled in ceramic package parts. Since destructive readout is essential for the $2T/2C$ ferroelectric memory, each part was used only once in the retention test to eliminate past history effects such as imprint.

2.2 Polarization measurement

Figure 1 shows typical polarization charge vs voltage loops of an SBTN capacitor that has been allowed to relax for about 5 s after poling, where P_s is the switched polarization charge from a capacitor in the up state, and P_{ns} is the non-switched polarization charge from a capacitor in the down state, both when a negative read voltage pulse is applied. In a $2T/2C$ ferroelectric memory cell, a voltage difference on a bitline pair corresponding to the

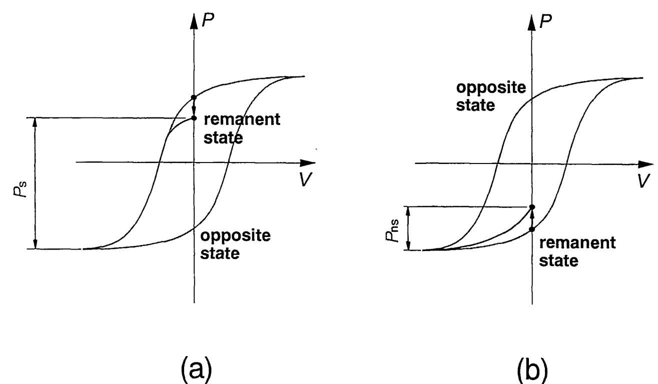

Fig. 1. Polarization charge vs voltage loops of an SBTN capacitor that has been allowed to relax for about 5 s after poling, where (a) P_s is the switched polarization charge from a capacitor in the up state, and (b) P_{ns} is the non-switched polarization charge from a capacitor in the down state, both when a negative read voltage pulse is applied.

transferred charge difference between P_s and P_{ns} is amplified to identify the memory logic state.[10] In the one transistor and one capacitor ($1T/1C$) cell architecture, the bitline voltage in terms of either P_s or P_{ns} is also compared with a reference voltage.[11] In the hysteresis loop, the nonvolatile component of the polarization is defined as $P_{nv} = P_s - P_{ns}$. In either memory cell configuration, P_{nv} must be greater than a specific value to prevent the sensing error of the bitline voltage difference with the sense amplifier.

For the transient polarization decay regime shorter than 530 ms, we monitored the change after poling in the output voltage from an operational amplifier with a linear capacitor which integrates the current from a poled ferroelectric capacitor in a Sawyer-Tower circuit,[12] yielding a voltage proportional to the amount of charge stored in the ferroelectric capacitor. Since there was a limitation in the duration of the transient polarization measurement, a pulse polarization measurement technique was used for the retention time exceeding 530 ms.

The pulse sequence used is shown in Fig. 2. The voltage pulses are triangular waves of ± 3 V with a duration of 11 ms. Switched and non-switched charges, P_s and P_{ns}, respectively, were measured as follows: (1) define the polarization state of a capacitor array with a cycle of negative and positive voltage pulses; (2) pole the capacitor array into the up state with a positive voltage pulse or the down state with a negative voltage pulse; (3) wait for about 5 s at room temperature for the initial polarization measurement; (4) read P_s from the capacitor in the up state and P_{ns} from the capacitor in the down state, both with a negative voltage pulse at room temperature; (5) repeat step 2 for rewrite; (6) store rewritten capacitors at room temperature for a selected period of retention time; and (7) repeat step 4 for retention measurements.

2.3 Memory retention test

Prior to storing test memory parts at high temperatures, a test data pattern was programmed (written) into each part at 2.43 V and 75°C. The programming voltage was chosen to be low enough, and the temperature was chosen to be the maximum for use in consumer applications. The programmed parts were then stored at temperatures of 125, 150, and 175°C for selected periods of retention time up to 2000 h. The baked parts were cooled to 75°C, and then their data integrity and functionality were tested at 2.43 V. Any memory part with failing bits was rejected. For each test condition of temperature and retention time, 10 test parts were used.

3. Results and Discussion

3.1 Polarization decay model

The polarization decay in SBTN capacitor arrays as a function of retention time is shown in Fig. 3. For the first 530 ms after poling, the values of P_{nv} were obtained from the transient polarization measurement. The initial pulse polarization measurement was made at 10 s and the values of P_{nv} at room temperature were approximately 12 μC/cm^2. The values of P_{nv} after 2- to 100-h retention times showed good agreement with those extrapolated with a straight line from the data set in the transient regime. It is therefore reasonable to extend the fitting line to 100 h and to explain the decay process in the short to long time regime (1 ms to 100 h) by a single decay mechanism. The linear dependence of the decay curve on logarithmic time yields a decay rate of 0.24 μC/cm^2 per decade. The logarithmic time dependence suggests that the polarization decay process has a distribution over orders of magnitude in relaxation time, and is described by[6–8]

$$P(t) = P_0 - m \log\left(\frac{t}{t_0}\right), \quad (1)$$

where t is the retention time, t_0 is the characteristic time at which the linear behavior of $P(t)$ begins with respect to $\log t$, P_0 is the polarization at $t = t_0$, and m is the decay rate.

3.2 Retention failure model

When the remanent polarization $P(t)$ decays with time t at a constant decay rate of $1/\tau$, $P(t)$ is expressed as

$$P(t) = P_0 \exp\left(-\frac{t}{\tau}\right), \quad (2)$$

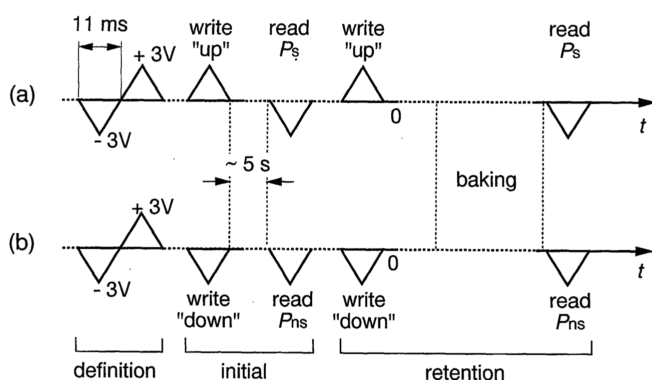

Fig. 2. Pulse sequences for polarization measurements. For the retention measurement, a positive voltage pulse sets the polarization state of a capacitor into (a) the up state and a negative voltage pulse sets it into (b) the down state. The amount of retained polarization charge after a selected period of retention time is determined with a negative voltage pulse for both states.

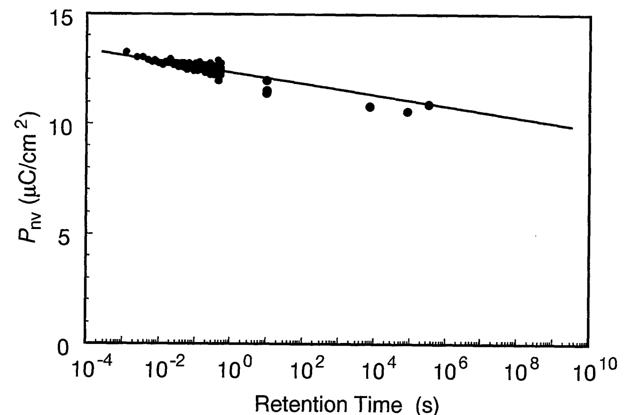

Fig. 3. Decay of P_{nv} in SBTN capacitor arrays at room temperature as a function of retention time. The fast decay of P_{nv} for the first 530 ms was observed by monitoring the integrated switching current. Evaluation of the long-term decay of P_{nv} was made by pulse polarization measurements.

where $P_0 = P(0)$, and $1/\tau$ is the rate constant for the decay. Let us assume that a memory device fails in a retention test when $P(t)$ of a memory capacitor reaches a specific value, P_f, which gives the lower limit of remanent polarization whose charge is detected by the sense amplifier. Then we have this expression for the time to failure t_f:

$$t_f = \tau \log\left(\frac{P_0}{P_f}\right). \tag{3}$$

In eq. (2), $1/\tau$ can be regarded as the specific decay rate determined by the polarization decay mechanism. The temperature dependence of the rate constant is then expressed as

$$\frac{1}{\tau} = \frac{1}{\tau_0}\exp\left(-\frac{E}{kT}\right), \tag{4}$$

where E is the specific activation energy, k is the Boltzmann constant, T is the absolute temperature, and $\tau = \tau_0$ at $E/kT = 0$. Combing eqs. (3) and (4), we obtain the following relationship between temperature and time to failure:

$$\log t_f = \frac{E}{kT} + \text{const.} \tag{5}$$

This relationship is commonly referred to as the Arrhenius reaction model and is adequate as far as eq. (2) is relevant to the decay process. However, the actual decay process is well described by eq. (1). Let us assume again that a memory device fails when $P(t)$ is equal to P_f. From eq. (1) this assumption leads to the following expression for time to failure:

$$\log\left(\frac{t_f}{t_0}\right) = \frac{1}{m}(P_0 - P_f). \tag{6}$$

If the slope m is regarded as the rate constant for the decay in remanent polarization given by eq. (1), it has a form analogous to eq. (4),

$$m = m_0 \exp\left(-\frac{E}{kT}\right), \tag{7}$$

where $m = m_0$ at $E/kT = 0$. From eqs. (6) and (7), we obtain the following relationship between temperature and time to failure:

$$\log\left[\log\left(\frac{t_f}{t_0}\right)\right] = \frac{E}{kT} + \text{const.} \tag{8}$$

Consequently, the temperature dependence of the time to failure in ferroelectric memories obeys the linear relationship between $\log(\log t_f)$ and $1/T$.

3.3 Retention failure distribution

The distribution of times to failure obtained from the temperature-accelerated retention test on 288-bit memory parts was approximated to a log-normal distribution, as shown in Fig. 4. This approximation indicates that memory retention failures occur when a threshold in remanent polarization P_f is reached. In this figure, cumulative failures apparently increase as the baking temperature is elevated, and tend to saturate with time. The saturation of cumulative failures at long retention times indicates a change in the failure mechanism and is a result of the lowering of the failure rate. Since the failure rate

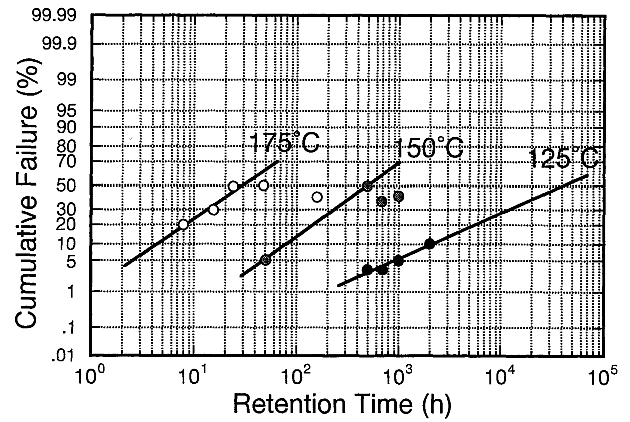

Fig. 4. Log-normal plot of cumulative failures for 288-bit memory parts at a write voltage of 2.43 V.

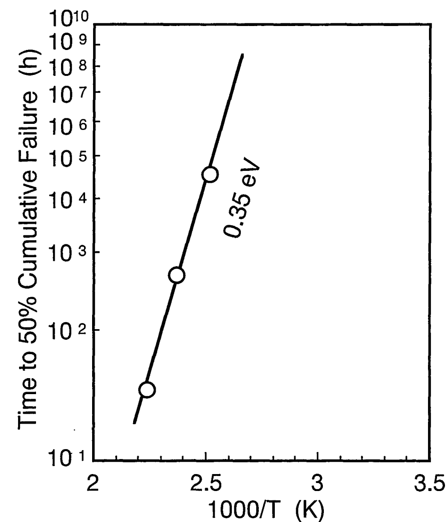

Fig. 5. Arrhenius plot to determine the activation energy for infant failures, showing a straight line with an activation energy of 0.35 eV.

in the saturated regime appeared to be stabilized, a random failure mechanism with a constant failure rate was adopted. Early failures during cumulative failures are rapidly increasing, on the other hand, were implicated in the relaxation process of remanent polarization described by eq. (1), because the logarithmic time dependence leads to a larger change in P_{nv} in the earlier part of retention time. Therefore, the infant failure regime is characterized by a rapid increase in cumulative failure and the failure distribution is approximated by fitting a straight line to the data set in the infant failure regime while cumulative failures are rapidly increasing.

Figure 5 shows the temperature dependence of the time to 50% cumulative failure in the infant failure regime. The best fit of the temperature dependence given by eq. (8) is obtained when the activation energy is 0.35 eV. Good linearity of the data in Fig. 5 supports the approximation that the decay in remanent polarization during the infant failure regime is governed by the logarithmic polarization decay process.

Since we assumed that the reliability of ferroelectric

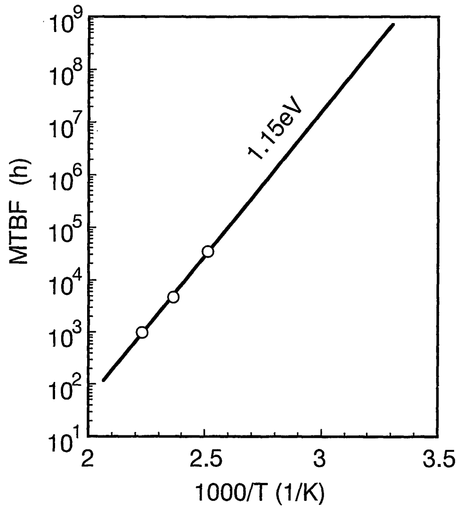

Fig. 6. Mean time between failures (MTBF) vs temperature to show a random failure mechanism with an activation energy of 1.15 eV. MTBFs were calculated using the χ^2 distribution with a 60% confidence level.

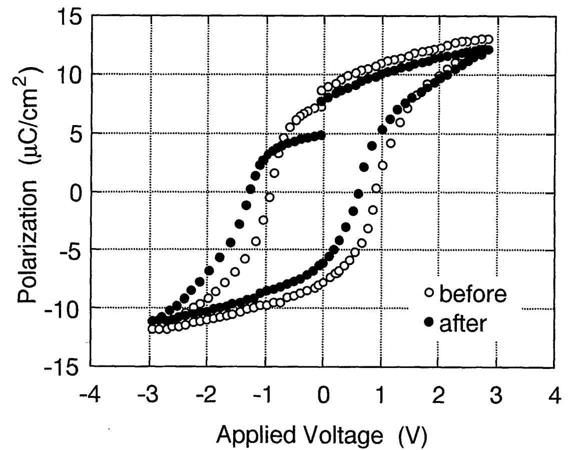

Fig. 7. Hysteresis curves of a SBTN capacitor array at 27°C, before and after storage at 125°C for 120 h.

memories in the saturated regime is characterized by a random failure mechanism, the temperature dependence given by eq. (5) was applied to the data set in this regime. In order to describe the failure times resulting from a random failure mechanism with a constant failure rate, we calculated the mean time between failures (MTBF) using the χ^2 distribution for a 60% confidence limit. The data used are the number of failing parts in the period of random failures with respect to the tested sample size for selected test durations at elevated temperatures, where infant failures are not included in the failure rate calculation. Figure 6 shows the temperature dependence of the MTBF. The fitting of the random failure model gives a straight line with an activation energy of 1.15 eV. This relationship can be used to predict the random failure rate at temperatures other than the test temperatures.

3.4 *Retention failure mechanism*

As demonstrated in the experimentally fabricated ferroelectric memories, there are two different mechanisms for memory retention failures. Using eq. (8), the activation energy associated with infant failures was calculated to be 0.35 eV. Once cumulative failures saturate, the memory retention failure is dominated by a random failure mechanism with an activation energy of 1.15 eV. The following argument deals with possible physical origins of these different failure mechanisms.

Let us first consider the infant failure mechanism, which follows the logarithmic time dependence of the polarization decay given by eq. (1). There are two possible origins of the logarithmic time dependence: the distribution of coercive energy responsible for polarization reversal and the distribution of trap depth responsible for space charge redistribution. In the former, the reversal of thermally fluctuating dipoles from one well to the other in the double-minimum potential with distributed coercive potential barrier height is responsible for the decay in remanent polarization. This process is stochastic and continues until thermal equilibrium is established. In the latter, redistribution of space charges due to the internal electric field and the concentration gradient influences the decay process. This process ends when the total energy is minimized. As a result of the redistribution, the polarization charge is effectively screened by space charges such as electrons and holes redistributed in traps.

Although either process can cause a change in remanent polarization with time, there is a marked difference between them. The thermal fluctuation process is reversible because the coercive energy distribution does not change with time. In contrast, the space charge redistribution process is irreversible, and as a result the final polarization state is memorized temporally. In ferroelectric materials, such memory effects are referred to as imprint,[13–15] which can be described as the establishment of a preference in polarization direction. As a result of imprint after storage at high temperatures, the hysteresis loop is no longer restored to the initial state. This distortion in the hysteresis loop is also observed in our SBTN capacitors, as shown in Fig. 7, and strongly implies that the polarization decay process is accompanied by imprint as a result of space charge redistribution. Another indication supporting the redistribution mechanism is the relatively small value of activation energy for infant failures obtained by applying the model following eq. (8). Robertson *et al.* suggested a similar value for the depth of electron and hole traps in bismuth-layered perovskites.[16] These shallow traps readily allow the redistribution of electrons and holes. We therefore conclude that the infant failure of the SBTN ferroelectric memory is caused by the redistribution of space charges in shallow traps. The time required for the space charge redistribution may depend on the defect density and stoichiometric deficiency in the film as well as storage temperature. It is therefore believed that there could be a distribution of trap depth, resulting in the logarithmic time dependence of the change in remanent polarization.

The random failure mechanism, in contrast, is characterized by a relatively high activation energy of 1.15 eV. In addition, microscopic failure analysis showed no distinct defects in failing capacitor elements. Since the

activation energy obtained is close to that for the motion of oxygen vacancies and/or ionic impurities in the ferroelectric,[15] the loss of polarization in failing capacitor elements is probably caused by the compensation or screening of the displacement dipole charges with mobile charges moving slowly at a certain rate determined by the activation energy. The memory retention failure rate in the random failure regime is therefore a function of the reaction rate of the mobile charges with displacement dipole charges and their concentration such as oxygen deficiency.

4. Conclusion

The temperature dependence of charge retention characteristics for integrated SBTN capacitors was studied. The SBTN capacitors were poled at 3 V and room temperature prior to the retention test. The remanent polarization decay at room temperature showed good linearity when plotted against logarithmic retention time over a wide range of 10^{-3}–10^{5} s. The logarithmic time dependence of the decay in remanent polarization was attributed to the distribution in trap depth responsible for the space charge redistribution leading to the irreversible change in resultant hysteresis loops. The temperature dependence of infant failures in a 288-bit $SrBi_2(Ta, Nb)_2O_9$ memory was fit to an empirical reliability model having a linear relationship between $\log(\log t_f)$ and $1/T$. Since this approximation yielded an activation energy of 0.35 eV similar to that of electron and hole traps in bismuth-layered perovskites and the process is irreversible, we believe that infant failures are associated with the redistribution of electrons and holes in shallow traps. Random failures, on the other hand, exhibited a low failure rate with an activation energy of 1.15 eV similar to that for oxygen vacancies and/or ionic impurities.

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