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Thermal Aging Effect in Poled Ferroelectric $SrBi_2(Ta,Nb)_2O_9$ Capacitors

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Changes in the electrical properties of poled ferroelectric $SrBi_2(Ta,Nb)_2O_9$ (SBTN) thin-film capacitors caused by high-temperature storage were studied. Current–voltage (J–V) characteristics of SBTN capacitors before and after high-temperature storage indicated that the current in SBTN is predominantly carried by electrons and limited by electrode interfaces. The voltage shift in the polarization–voltage (P–V) curve caused at high temperatures was ascribed to a bulk effect because there were no definite changes in the interface-limited J–V characteristics before and after high-temperature storage. Assuming the pinning of domains by capturing electrons emitted from traps distributed in the energy gap, we describe the decay in switchable polarization with the power of time. The activation energy for the decay in switchable polarization associated with electron capture was determined to be 0.23 eV based on the temperature dependence of the decay in switchable polarization.

KEYWORDS: ferroelectric, $SrBi_2(Ta,Nb)_2O_9$, imprint, pinning

1. Introduction

In nonvolatile ferroelectric memories, the number of write/read cycles without polarization fatigue (the endurance) and the data integrity without power supply are the most critical reliability concerns. In recent years, bismuth-layered structure ferroelectrics, such as $SrBi_2Ta_2O_9$ (SBT) and $SrBi_2(Ta,Nb)_2O_9$ (SBTN), have demonstrated excellent endurance performance by exceeding 10^{12} cycles.[1–6] In contrast, temperature effects on the data integrity remain as a nonvolatile-memory-specific issue. When assessing the reliability performances related to the data integrity of ferroelectric memories, one should take into account the following two aging effects observed during a given retention period: (1) relaxation and (2) imprint. Relaxation is characterized by the decay in retained polarization over a long period of time, which is frequently termed relaxation.[7–12] Imprint, on the other hand, is characterized by the loss of switchable polarization from a preliminarily poled remanent state to the opposite (complementary) remanent state, resulting from the establishment of a preference for the preliminarily poled remanent state over the opposite remanent state during storage or unipolar voltage pulsing.[13–17] Once imprint has occurred, a voltage offset appears in the polarization–voltage (P–V) hysteresis curve with increasing the coercive voltage from the preliminarily poled remanent state to the opposite remanent state. As a result, the remanent polarization of the opposite remanent state is decreased. Thus, imprint is implicated in the loss of switchable polarization from a preliminarily poled remanent state and is ascribed to the pinning of domains by charge carriers at pinning centers.[18] Early studies on $BaTiO_3$ and $Pb(Zr,Ti)O_3$ (PZT) bulks have explained the origin of the asymmetry in the P–V hysteresis curve by the space charge effect.[19,20] Similar reasoning has been adopted in the internal field development of PZT and $(Pb,La)(Zr,Ti)O_3$ (PLZT) thin films in terms of asymmetric distributions of electrons and oxygen vacancies.[17,21–23] Although these aging processes have been described using empirical expressions,[15,16,24,25] the origin of the time evolution and the temperature dependence of the decay in switchable polarization have not been explored.

In this study, we will examine thermal effects on the switchable polarization of SBTN capacitors. In order to determine the type of charge carrier in SBTN, the bias voltage dependence of the leakage current in SBTN capacitors is studied. With an assumption of carrier emission from traps distributed in the energy gap, an analytical model which accounts for the temperature effect on imprint in ferroelectric capacitors is introduced. Based on this model, the activation energy responsible for imprint in SBTN capacitors is inferred from the temperature dependence of the decay in switchable polarization which can be observed in deformed hysteresis curves.

2. Experiment

2.1 Sample preparation

In the present experiments, 240-nm-thick SBTN capacitors were prepared by metal-organic decomposition processing on Pt-deposited silicon wafers with integrated metal-oxide-silicon devices for driving ferroelectric memories, followed by annealing at a high temperature in atmospheric oxygen.[5] After deposition of the top Pt electrode on top of the ferroelectric layer, and subsequent patterning of 110 capacitor arrays with the top electrode size of $5 \times 5\,\mu m^2$ each for accurate measurement of the polarization charge, the wafers with capacitors have experienced the interlayer dielectric deposition, metallization, and passivation processes necessary for ferroelectric memory fabrication. Finally, the test capacitor arrays were mounted in ceramic packages.

2.2 J–V measurement procedure

Current–voltage (J–V) characteristics of poled SBTN capacitors were observed before and after storage at high temperatures. Prior to J–V measurements, SBTN capacitors were positively poled to the top electrode with a voltage pulse of 3 V at room temperature. Then the J–V measurements on poled capacitors were made every 0.1 s after each 0.1 V applied voltage increment, from 0 to 5 V, and after each 0.1 V applied voltage decrement, from 0 to -5 V. After the initial J–V measurements, the test capacitors were again positively poled to the top electrode with a voltage pulse of 3 V at room temperature and subsequently stored at 125°C for 100 h. After high-temperature storage, J–V measurements were also made on the test capacitors in the same manner. An HP-4145B semiconductor parameter analyzer was used for the measurements.

2.3 Imprint test procedure

To examine the nonvolatility in hysteresis loops, we made pulse polarization measurements as part of retention testing.[25] For instance, when a ferroelectric capacitor has been poled into one of the two possible states, and subsequently stored at an elevated temperature for a selected period of time, a voltage offset in the P–V hysteresis loop appears due to the preference for the up state over the down state. Imprint effects on the switchable polarization are then examined by measuring switched and nonswitched polarizations for the opposite state to the poled state for remanence, denoted by P_s and P_{ns}, respectively, and the voltage offset in the P–V hysteresis loop. As in the two-transistor and two-capacitor ($2T/2C$) memory cell, a certain amount of difference between P_s and P_{ns}, at least 1 μC/cm^2 typically, is required for discriminating the two logic states, logic "0" and logic "1". We examined the imprint effect on the switchable polarization in terms of the polarization difference defined by

$$P_{nv} = P_s - P_{ns}, \tag{1}$$

for the opposite state. Test sample packages, containing capacitors poled into known states, were subjected to elevated temperatures of 75, 125, and 150°C for up to 100 h. Pulse polarization measurements were made at room temperature before and after high-temperature storage using triangular voltage pulses of ±3 V with a duration of 11 ms.

3. Result and Discussion

3.1 Imprint effect on J–V characteristics

Figure 1 shows typical J–V curves for a positively poled SBTN capacitor before and after storage at 125°C for 100 h. The forward currents before and after high-temperature storage are identical. For the reverse currents, on the other hand, there appears a voltage shift of approximately 0.2 V between the anomalous current peaks due to polarization reversal. This voltage shift is a direct result of imprint and therefore agrees with the change in the coercive voltage in the P–V curve, as shown in Fig. 2. At high reverse voltages (<-2 V), the reverse currents before and after high-temperature storage are also identical. These J–V characteristics indicate that as a result of high-temperature storage there is no change in the spatial distribution of carriers leading to a change in the current transport in ferroelectric capacitors.[26] However, SBTN capacitors exhibit definite imprint effects. This finding suggests that imprint is a localized effect in the ferroelectric capacitor. The asymmetry in the J–V curves at high voltages (>2 V and <-2 V) is strongly related to the type of majority carrier in the ferroelectric capacitor and is ascribed to the interfacial asymmetry when current transport is limited by electrode interfaces. The low forward currents at high forward voltages and high reverse currents at high reverse voltages indicate that electron injection is significant at the top electrode interface due to the interfacial irregularity associated with the surface roughness as a result of grain growth.[27] Thus, we believe that electrons are the majority carriers in the SBTN capacitors.

3.2 Decay in switchable polarization

Hence, we consider a metal-ferroelectric-metal capacitor with an external bias source. When the ferroelectric capacitor is poled by applying a field, a remanent (spontaneous) polarization appears along the applied field in the ferroelectric capacitor even after the field is removed. If both metal electrodes are grounded after poling, the depolarization field due to polarization charges is equal to opposed external field due to the compensating electrode charges, so that the macroscopic field in the ferroelectric capacitor is zero at any time. Therefore, it appears that there are no macroscopic electric fields which cause a change in polarization of the ferroelectric capacitor. Nevertheless, ferroelectric capacitors exhibit an aging effect characterized by the decay in switchable polarization caused by high-temperature storage.[14,25] This fact suggests that the imprint phenomenon is a manifestation of microscopic changes in the charge distribution of the ferroelectric capacitor.

Slow changes of the charge distribution which take a long time have been attributed to carrier emission into the conduction band from localized traps distributed in the insulating energy gap.[28] If the number of traps lying in a narrow range of energy between E and $E + \mathrm{d}E$ per unit volume is given by $g(E)\mathrm{d}E$, we have

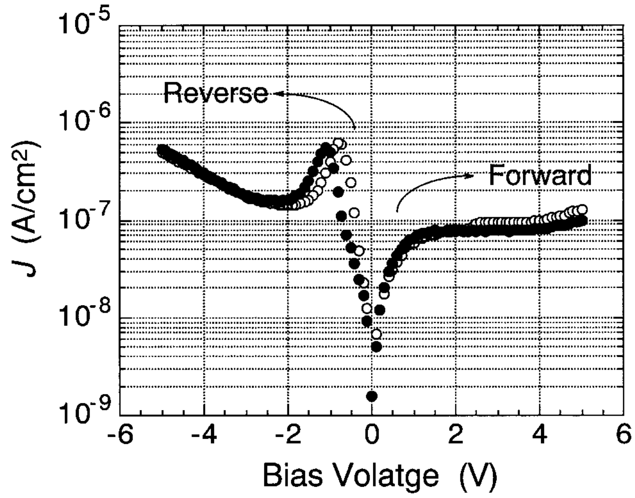

Fig. 1. Changes in the leakage current for a positively poled SBTN capacitor before (●) and after (○) storage at 125°C for 100 h. The forward current measurement was followed by the reverse current measurement at room temperature.

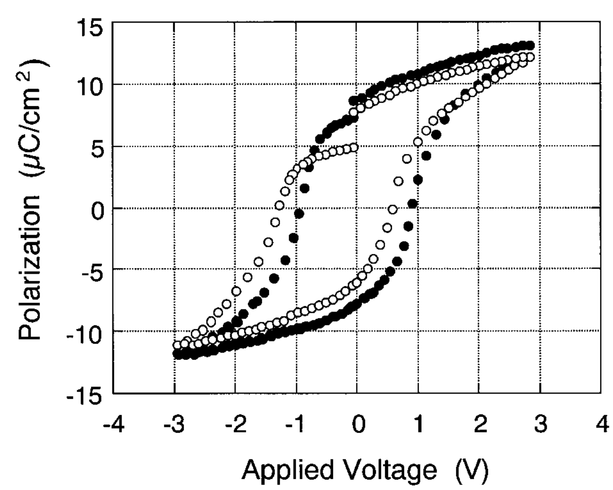

Fig. 2. Typical P–V hysteresis curve for positively poled SBTN capacitors before (●) and after (○) storage at 125°C for 100 h, obtained by pulsed polarization measurements.

$$\int_0^{\infty} g(E)\,\mathrm{d}E = N, \tag{2}$$

where E is the energy depth from the bottom of the conduction band, $g(E)$ is the distribution function of traps per unit volume, and N is the total number of traps per unit volume. The number of electrons emitted from traps lying between E and $E + \mathrm{d}E$ during a short time interval between t and $t + \mathrm{d}t$ is proportional to the number of these traps, i.e.,

$$r(t)\,\mathrm{d}t = \alpha g(E)\,\mathrm{d}E, \tag{3}$$

where $r(t)$ is the rate of electron emission from traps at an energy level of E per unit time and α is a constant. If the rate of electron emission from these traps into the conduction band is dependent on the energy depth, the waiting time t for the occurrence of electron emission from a trap at an energy depth of E is given by[29]

$$\frac{1}{t} = \nu_0 \exp\left(-\frac{E}{kT}\right), \tag{4}$$

where ν_0 is the vibration frequency of trapped electrons, k is the Boltzmann constant, and T is the absolute temperature. From eqs. (3) and (4), we have

$$r(t) = \alpha kTg(E)\frac{1}{t}. \tag{5}$$

Then the rate of electron emission from entire traps distributed in the energy gap $R(t)$ is given by

$$R(t) = \int_0^{\infty} r(t)\,\mathrm{d}E = \alpha NkT\frac{1}{t}. \tag{6}$$

It is immediately noticeable that $R(t)$ is independent of $g(E)$.

Here, we assume that domain pinning centers are distributed in the ferroelectric capacitor in a random manner. The pinning centers capture encountered electrons at a constant rate. In addition, we assume in the following that a certain amount of switchable polarization is reduced by capturing an electron by a pinning center. Under this condition, the variation in P_{nv} with time follows

$$\frac{\mathrm{d}P_{\mathrm{nv}}(t)}{\mathrm{d}t} = -\beta R(t)P_{\mathrm{nv}}(t), \tag{7}$$

where β is a proportionality constant associated with electron capture. Substituting eq. (6) into eq. (7), we have the solution of eq. (7) for a long period of time between t_0 and t:

$$P_{\mathrm{nv}}(t) = P_0\left(\frac{t}{t_0}\right)^{-m}, \tag{8}$$

where $P_0 = P_{\mathrm{nv}}(t_0)$ and

$$m = \alpha\beta NkT. \tag{9}$$

This deduction can be confirmed by scattering the retention test data in a log P_{nv} versus log t plot, as shown in Fig. 3. The slopes of the lines of best fit are essentially constant with respect to log t and yield the values of m corresponding to storage temperatures of 75, 100, and 125°C, respectively, showing that the value of m is exponentially rather than linearly dependent on the temperature (Fig. 4). This consequence can be explained by making the further assumption that an electron approaching a pinning center must overcome a barrier of E_{a} in order to be captured.[30] Then, the coefficients $\alpha\beta$ in eq. (9) are proportional to $\exp(-E_{\mathrm{a}}/kT)$ because β in eq. (7) is related to the electron capture rate of the pinning center. The pre-exponential coefficient kT in eq. (9) is then regarded as a constant, with respect to the abrupt change in $\exp(-E_{\mathrm{a}}/kT)$ with temperature.

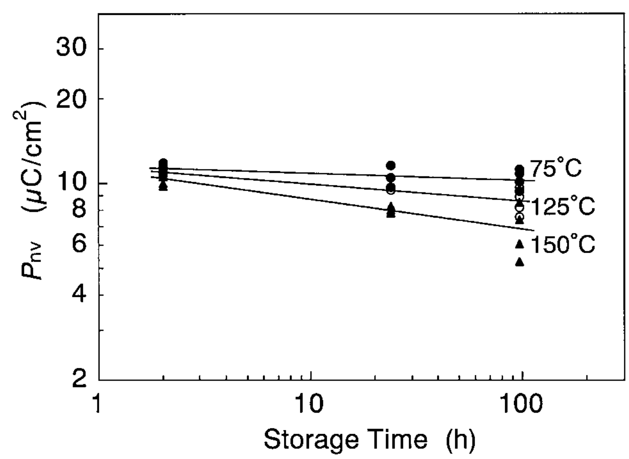

Fig. 3. P_{nv} ($= P_{\mathrm{s}} - P_{\mathrm{ns}}$) of $SrBi_2(Ta,Nb)_2O_9$ capacitors switched into the opposite remanent state after high-temperature storage. (P_{s}) Switched polarization acquired from a capacitor in the up state. (P_{ns}) Nonswitched polarization acquired from a capacitor in the down state.

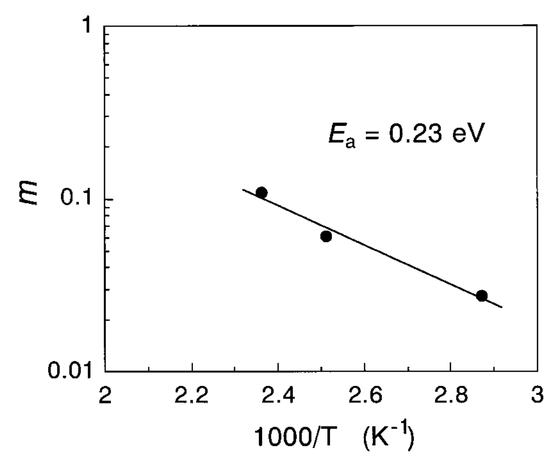

Fig. 4. Temperature dependence of the decay rate of switchable polarization for the opposite remanent state against a poled remanent state, showing an activation energy of 0.23 eV for thermal imprint.

$$m = \gamma N \exp\left(-\frac{E_{\mathrm{a}}}{kT}\right), \tag{10}$$

where γ is a constant. With this approximation, the activation energy of $E_{\mathrm{a}} = 0.23$ eV is obtained from the slope of the line of best fit in Fig. 4.

Although the activation energy was calculated from the temperature dependence of the decay in switchable polarization following the power of time, the behavior during a long period of time is quite similar to that described by an empirically accepted expression following the logarithm of time,[8–11,25]

$$P_{\mathrm{nv}}(t) = P_0 - m^* \log\left(\frac{t}{t_0}\right), \tag{11}$$

where $m^* = m_0 \exp(-E_{\mathrm{a}}/kT)$ and m_0 is a constant. In fact, the value of E_{a} obtained from the fitting of eq. (11) is calculated to be 0.19 eV, which is close to that obtained above. These small values of the activation energy for the electron capture process in SBTN imply a low overlap energy between the periodic lattice potential and the trap potential of pinning centers. Unexpectedly, these values are also close to those obtained from the temperature dependence of infant retention failure times for SBTN ferroelectric memories (0.35 eV).[25) The similar activation energy responsible for retention leads us to believe that relaxation in SBTN is also related to the electron capture process by pinning centers. A possible explanation is that emitted electrons are captured by preferred pinning centers to screen or compensate the polarization charges as well as to pin the domains. This argument leads to a comprehensive understanding of imprint to be a result of the redistribution of emitted electrons, and also agrees with the deduction in our previous report that the relaxation in remanent polarization is due to the redistribution of carriers rather than polarization reversal.[28) However, it should be noted that such redistribution of carriers must be highly localized because J–V characteristics before and after high-temperature storage indicate that there is no macroscopic change in the entire charge distribution throughout the capacitor during the thermal aging process.

4. Conclusion

Current–voltage (J–V) characteristics of $SrBi_2(Ta,Nb)_2O_9$ capacitors before and after high-temperature storage indicated that carriers in SBTN are electrons and that imprint is a localized effect. An analytical model of the thermal aging process in poled ferroelectric thin-film capacitors was introduced. The decay in switchable polarization with the power of time originates from the emission of electrons from traps distributed in the energy gap, while the exponential temperature dependence arises from the electron capture process associated with pinning centers. Based on this model, the temperature effect on the decay in switchable polarization was analyzed using high-temperature storage test data for SBTN capacitors. The temperature dependence of the decay in switchable polarization provided a thermal activation energy of 0.23 eV. Considering the role of thermally emitted electrons from traps, it was emphasized that the redistribution of electrons is responsible for both imprint and relaxation processes in SBTN capacitors.

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