Integrated Ferroelectrics, 1999, Vol. 27, pp. 291-314
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Advanced LSI Embedded with FeRAM for Contactless IC Cards and its Manufacturing Technology

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(Received March 7, 1999)

High performance LSIs embedded with ferroelectric random access memory (FeRAM) for contactless IC cards are now commercially available. The emphasis is placed on the materials solution with $SrBi_2(Ta,Nb)_2O_9$ (SBTN) which enables to exploit the potential performance of FeRAMs for composite logic/microcontroller LSIs operating at high speeds and low powers. The leading-edge 0.6-μm and double-level-metal FeRAM technology produces microcontroller-embedded LSIs with 14-kbit or 64-kbit FeRAM. A mature 0.8-μm and single-level-metal process has been built to maximize the die yield. Yields exceeding 90% indicate the excellent process stability. Product qualification data have proven the robust FeRAM technologies.

Keywords: ferroelectric memory; embedded LSI; $SrBi_2(Ta; Nb)_2O_9$; contactless IC card

INTRODUCTION

As the transmission distance between an RF-powered contactless IC card and the reader/writer unit is extended under a limited RF power, the driving power available for the passive LSI in the IC card is decreased. In addition, the transaction time becomes the most significant bottleneck in mobile IC card applications. This bottleneck commonly arises from the performance, e.g., operation speed, power consumption, etc., of nonvolatile memories incorporated in the LSIs. For instance, a 4-kbit EEPROM, a typical nonvolatile memory, needs more than miliseconds, meanwhile it dissipates miliwatts for an erase/write (update) operation of one byte data. One of the solutions to address this bottleneck is the use of ferroelectric random access memory (FeRAM) based on strontium bismuth tantatlate-niobate ($SrBi_2(Ta,Nb)_2O_9$; SBTN) having a bismuth-layered perovskite structure.[1,2] As is expected, recent efforts to merge SBTN-based FeRAMs into logic or microcontroller LSIs have provided high-performance embedded LSIs which well meet the requirements from conactless applications.[3,4] The FeRAMs in these LSIs are capable of write/read operations dissipating extremely low powers of the order of microwatts and exceeding 10^{10} cycles at temperatures from -10 to 70 °C for consumer applications and from -10 to 85 °C for industrial applications. The data retention failure rate is expected to be less than 10 FITs under use conditions.

In this paper, we overview the latest advances in FeRAM technologies applicable to embedded LSIs for contactless identification and electronic commerce. Following a brief description of embedded LSI architectures featuring FeRAM performances, typical issues in

ferroelectric fabrication processes are discussed. The degree of a built process capable of 0.8 μm lines and spaces is rated from the fabrication yield of an embedded LSI with 1-kbit FeRAM for contactless identification. Typical yield limiting factors in the ferroelectric backend process are discussed. Finally, the data retention ability of FeRAMs using SBTN against environmental disturbances, such as temperature, x-ray, and radio wave fields is examined.

CONTACTLESS APPLICATIONS

Systems-on-chips are integrating more functions with the increment of both the operation speed and packing density. Contactless IC cards are such leading-edge products for identification and electronic commerce. As we demonstrated in experimentally fabricated logic and microcontroller LSIs,[3-5] FeRAM is the best choice for the nonvolatile memory to be merged in such LSIs because of its advantages in write/read speed and operation power as well as in write/read endurance. A typical operation voltage range as a function of access time for an experimentally fabricated 256-kbit FeRAM using $SrBi_2Ta_2O_9$ (SBT) is shown in Fig. 1.[6] The SBT-based FeRAM ensures the fast access time (< 200s) at low operation voltages (< 3V).

In contactless IC card applications, several RF modulation/ demodulation schemes are used. Due to the superior noise immunity, low carrier frequencies, e.g. 125 kHz, are good enough for low data transmission rate applications (~10 kbps), while the card requires a coiled antenna in many turns with an additional coupling capacitor. Since the amount of data to be transmitted are limited, a 288-bit FeRAM fabricated

from SBT has been incorporated in a logic LSI operating at 125 kHz and 7.8 kbps by binary phase shift keying (BPSK).[3]

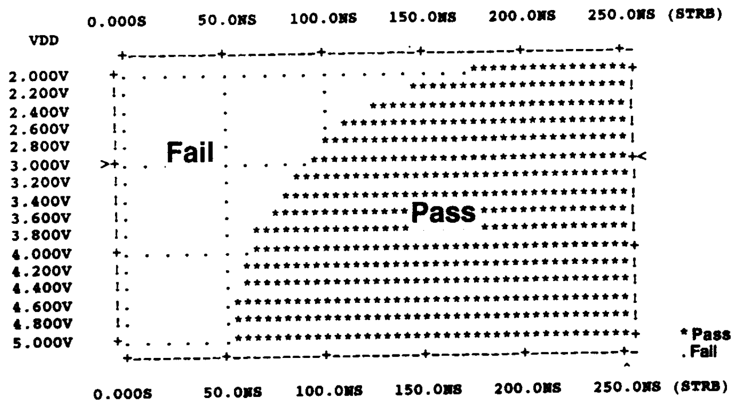

FIGURE 1 Operation voltage range *vs.* access time for an SBT-based 256-kbit FeRAM.[6]

Higher carrier frequencies are preferred for high data transmission rate applications, while the noise interference effect becomes significant as the carrier frequency is increased. Figure 2 shows a 1-kbit-FeRAM-merged logic LSI developed for 13.56 MHz application. The die dimensions are 1.8 x 2.5 mm^2 and the thickness is reduced to 180 μm for use in 700-μm-thick contactless IC cards. The system is comprised of an analog front-end (a power generator, power-on reset, clock generator, modulator, etc.), a control logic, and a 1-kbit FeRAM. The power generation circuitry generates the DC supply voltage by rectifying the 13.56-MHz power signal received with turned resonant circuits connected

to the LSI. The data packet is transmitted from the reader/writer unit at a rate of 212 kbps modulated on the power signal by amplitude shift keying (ASK). The LSI responds to the inquiry from the reader/writer unit at the same data transmission rate using binary phase shift keying (BPSK) modulation at 848 kHz. This product is fabricated with a single-metal, single-poly and 0.8-μm COMS technology.[7]

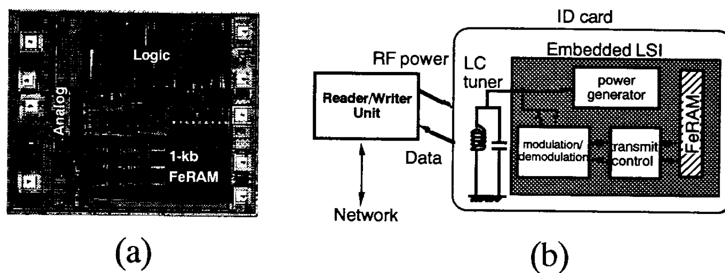

FIGURE 2 (a) An embedded LSI with a 1-kbit FeRAM for 13.56 MHz RF identification and (b) a block diagram of the ID system.

In advanced contactless IC cards for electronic commerce, data security is a potential concern. One of the effective solutions to this problem is the use of systems-on-chips involving a microcontroller unit (MCU) with a captive logic or co-processor capable of cryptographic data processing. The latest commutation IC card uses an 8-bit MPU-embedded LSI with a 14-kbit FeRAM provided with a double metal, single-poly and 0.6-μm CMOS technology. The LSI has a cryptograph logic circuitry based on the DES (data encryption standard) and can address anti-

collisional communications among plural cards. The carrier frequency is 13.56 MHz and the communication protcol follows the ISO14443 regulation. The IC card can reach the reader/writer unit from 10 cm away.

More advanced systems-on-chips integrate reconfigurable logic, instead of captive co-processors, to address many different algorithms for cryptographic data processing. However it takes a time to reconfigure the separated logic blocks sequentially. To cut the reconfiguration time, we proposed a distributed logic array architecture with many local array elements (Fig.3).[8] Each array element has an FeRAM holding logic circuit patterns. When a reconfiguration command is executed, the logic in every element is changed simultaneously.

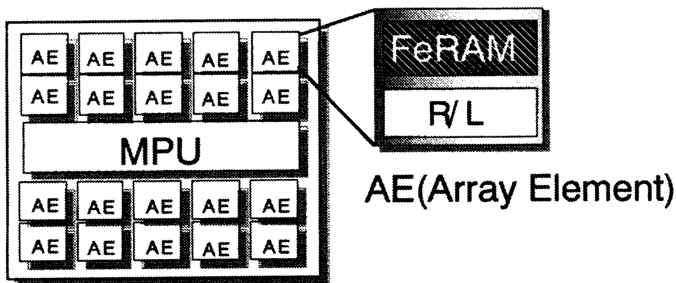

FIGURE 3 A distributed logic array architecture for fast reconfiguration.

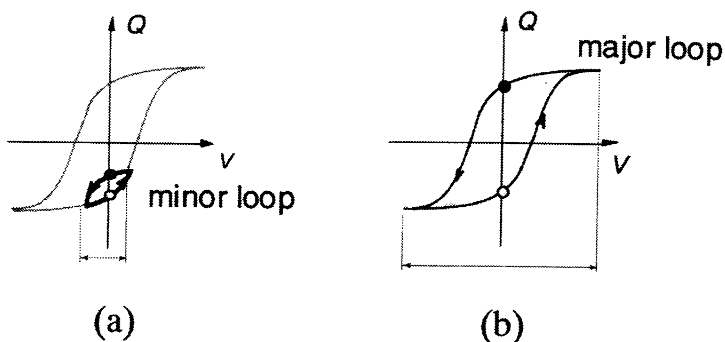

FIGURE 4 (a) A memory operation mode at lower voltages when the system is working and (b) another memory operation mode at higher voltages before the system shut-down.

A low-power operation of FeRAMs is due to the introduction of a multi-mode memory operation, according to the system status.[8] When the system is working, every data in the FeRAM is considered to be temporal. This allows the storing of data on the minor loop of the hysteresis (Fig. 4 (a)) and saves the operating power. When the system is being shut-down, every data is stored on the major loop of the hysteresis in order to secure the data retention (Fig. 4(b)). Consequently, with low power and high speed FeRAM circuit technologies, it is expected that the duration of a reconfiguration update is halved and the total power is saved by 30 %.[8]

WAFER FABRICATION PROCESS

Reliability of integrated ferroelectric capacitors is strongly dependent on the wafer fabrication process. First of all, high-quality ferroelectric thin films must be grown on electrode plates. Any defects, imperfect crystallinity, or off-stoichiometry induced in the films during wafer fabrication processing are sure to cause an increase in leakage current, low dielectric constant, and/or poor ferroelectricity. Secondly, optimum choices and combinations of ferroelectric materials, electrode materials, and insulating materials are of necessity for ensuring the reliability of integrated ferroelectric capacitors. Finally, even though the ferroelectric materials exhibit good intrinsic electrical properties, it is more important that those properties can be maintained and controlled throughout the fabrication process. These integration issues certainly arise from ignorance of the relationships between ferroelectric material properties and silicon process technologies. For instance, there are many causes of damage in ferroelectric processing, such as forming, annealing, and plasma etching.[9,10] It is therefore a crucial issue for FeRAM manufacturers to understand these relationships and develop key techniques to provide less-damaged ferroelectric memory capacitors. The authors expect that some of these issues can be solved with the following approaches.

Film Formation Techniques

The metal-organic decomposition (MOD) technique is preferable for growing ferroelectric thin films for low-density memories with films of typically 150 - 200 nm in thickness. Ferroelectric thin films are deposited

on the substrate by spin-on coating of a homogeneous solution containing the stoichiometry correct precursors with subsequent drying and annealing for crystallization.[11] The spin-on technique allows low machine overhead for manufacturing the integrated ferroelectric devices as well as stoichiometry correct films. This mature technique has been applied to the 6-inch wafer fabrication. Keeping the advantages of the MOD technique, we introduced a liquid source misted chemical deposition (LSMCD) technique using similar MOD liquid precursors.[12] This technique is capable of unlimited choice of liquid precursor materials and no need for further composition control during the deposition at room temperature. Recent improvements in the mist carrier system resulted in the formation of finer particles misted from octane based MOD type SBT solution.[13] Figure 5 shows a resultant SBT film formed on trenches with sub-micron lines and spaces, whose feature size is applicable to mega-bit scale FeRAMs.

For further densification of FeRAMs, stacked ferroelectric memory cell structures will be demanded. Then the ferroelectric capacitors need to be formed on the CMOS substrate planarized by chemical mechanical polishing (CMP). In addition, the lowering of film growth temperature is required to prevent silicide sheet resistance and contact resistance from varying during high temperature annealing. In practice, the film growth temperature must be lower than 650 °C to maintain the silicide sheet resistance at lower levels than the channel resistance of access gate transistors. A chemical modification of MOD precursor may be effective to lower the crystallization temperature.[14]

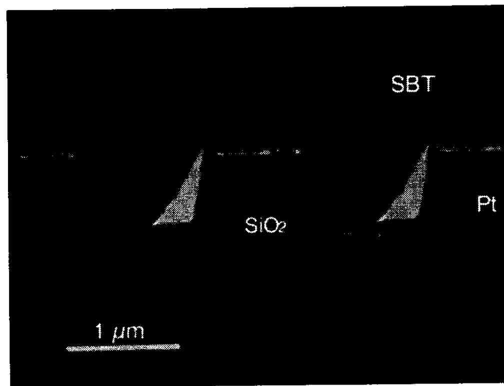

FIGURE 5 Ultra-thin SBT film formed on sub-micron trenches by LSMCD.

Patterning of Ferroelectric Capacitors

Since ferroelectric materials of metal-oxide ferroelectrics and platinum for the electrode are chemically stable, it is essentially difficult to obtain fine patterns by chemical wet and/or dry etching.[15] Although ion milling is one of the widely used patterning techniques, the high energy ion bombardment causes serious damage to underlying MOS transistors and leaves nonvolatile platinum compound residue on sidewalls of the photoresist, resulting in the formation of fences on capacitors. In addition, the poor etch selectivity to the underlying materials causes non-uniform patterning of capacitors over the wafer surface.

To obtain better ferroelectric to Pt and Pt to SiO_2 etch selectivities, we examined a variety of halide mixtures for magnetron reactive ion etching (RIE) and found that some of chlorine-based mixtures are effective for

etching of these materials using photo-resists.[16] Figure 6 shows a cross sectional micrograph of a planar memory cell with a ferroelectric capacitor fabricated with a RIE machine, which demonstrates the highly selective RIE technology without undercutting of the SiO_2 layer under the SBTN/Pt layers. Platinum and SBTN etch rates are both from 100 to 200 nm/min with sufficient selectivities. With a proper choice of process gases and etching conditions, the RIE will challenge the sub-half micron range (< 0.25 μm) in feature size required for megabit-scale FeRAM fabrication.

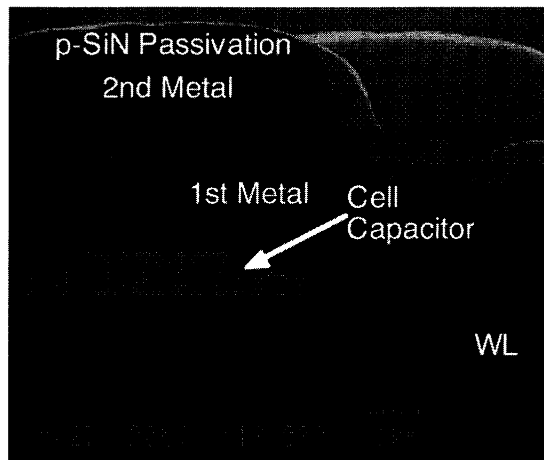

FIGURE 6 A cross sectional view of a FeRAM cell using a double level metal technology.

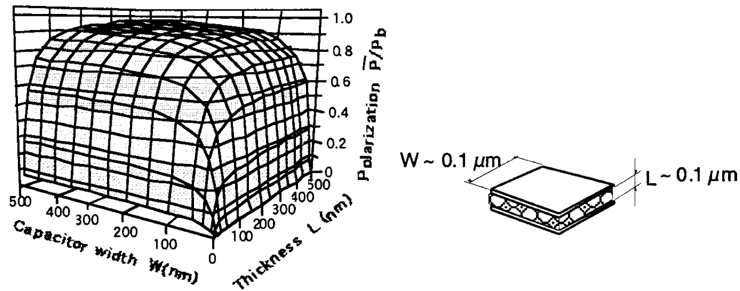

FIGURE 7 A 3-D profile of the remanent polarization of SBTN capacitors reduced to that of bulk.

The critical dimensions of the ferroelectric capacitor were estimated from the thermodynamic phenomenological theory considering the depolarization effect in the ferroelectric and the surface diminution effect of long rage forces.[17] The calculation shows that minute SBTN capacitors work well as small as 0.1 μm in width and 0.1 μm in thickness (Fig. 7). These physical dimensions allow the design of megabit-scale FeRAMs with the feature size below 0.15 μm.

Process Damage

A common concern for plasma processes is the sensitivity of bismuth-layered perovskites to hydrogen containing atmosphere.[18] In the ferroelectric backend process, hydrogen chemicals are used in chemical vapor deposition (CVD) of SiO_2 dielectric or SiN_x passivation layers and contact etching. In many cases, recovery of hydrogen damage can be achieved by oxygen anneals. However, post-anneals sometimes cause further degradation of ferroelectric capacitors when the deposited layers

contain excess hydrogen. On the other hand, hydrogen is sometimes required to restore the damaged MOS transistors. Consequently, the process window becomes very small. In order to restore the damaged MOS transistors by annealing without degrading ferroelectric capacitors, dummy metals are placed on the ferroelectric capacitors using the second metal layer.[19] The penetration of hydrogen into the ferroelectric capacitors is effectively prevented in the presence of the dummy metals.

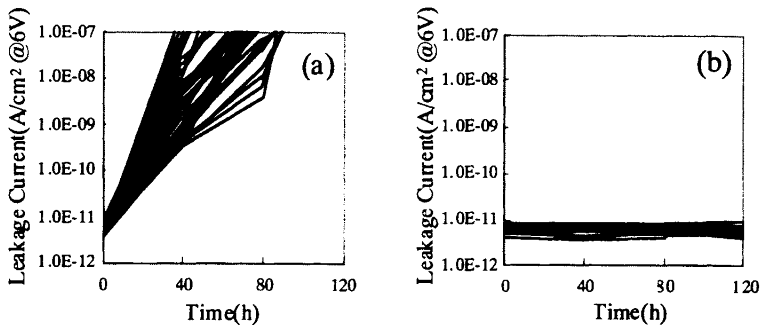

FIGURE 8 Leakage current *vs*. stress time in the presence of 85% RH moisture for SBT capacitors with (a) a SiO_2 passivation layer and (b) a SiN_x passivation layer, respectively.

Due to the similar reason, not plasma deposited SiN_x but SiO_2 has been used for the passivation material of FeRAMs with hermetic packages made of ceramics against moisture ingression. When a plastic package is required, however, moisture resistance at the surface of the die must be considered. With many improvements in dehydration treatment, it was

found that SiN_x is available for the surface of the die without degrading the underlying ferroelectric capacitors. Figure 8 compares the behaviors of leakage current in SBT memory capacitors with SiO_2 and SiN_x on each top during an unsaturated pressure cook bias temperature (USPCBT) test. The SBT capacitors with SiN_x exhibit no resistance degradation, so that the use of plastic packages is allowed for FeRAM.

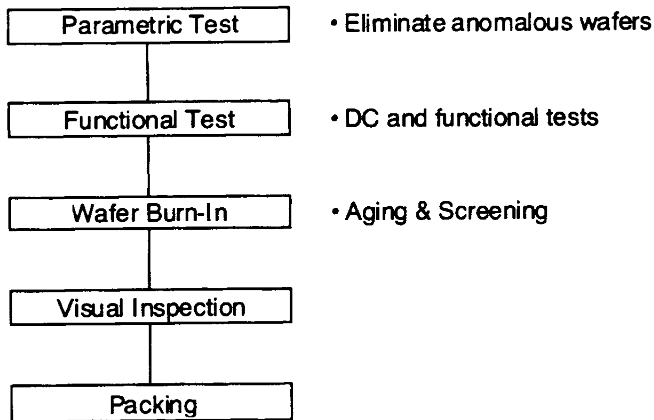

FIGURE 9 A typical wafer test flow for embedded LSIs with FeRAM.

Wafer Probe Test

Finished wafers are probed for parametric and functional tests. Parametric tests are performed on each wafer with parametric test structures to eliminate the wafers whose die performance falls outside the tolerance limits. Subsequently, every die is electrically probed to detect errors in its

DC characteristics and logic, analog, and memory functions. After the probe test, in general, good dies are packaged and final functional tests are performed on each at elevated temperatures before shipping to reject anomalous and marginal dies from the die population and to screen out potentially defective dies. However, embedded LSIs for IC card applications need to be shipped in wafer form in accordance with customer's requirements. Accordingly, a wafer burn-in technique is required. Figure 9 shows a typical wafer test flow for logic LSIs incorporating FeRAMs. Wafer bake is carried out to accelerate the relaxation of remanent polarization in ferroelectric memory capacitors. In addition to the relaxation effect, this test is used to detect mechanical reliability problems (e.g., interconnect integrity) and dielectric breakdown. From known relations between stress and time-to-failure, the wafer burn-in condition is determined to eliminate nearly all the infant failures. Finally, the dies on wafer are visually inspected to reject mechanical defects before shipping.

FABRICATION YIELD

In FeRAMs, the most yield limiting mechanism is a point defect as commonly seen in CMOS fabrication. Product yield for a given die size will primarily be a function of average defect densities in the wafer fab (which in turn depends on particle counts, handling problems, etc.). Failures can also result from excessive parametric variation in the process, especially when the design includes specific circuitry sensitive to the variations in process parameters. Therefore yield improvement efforts on FeRAM fabrication are also aimed at controlling the process parameters as

well as monitoring and reducing point defect density levels. The controlling of process parameters is associated with the line yield, which can be defined as the ratio of unprocessed wafers in to processed wafers out. The final acceptance of processed wafers is made by performing parametric measurements on the test structures located at selected die sites on the wafer. The average point defect density in the wafer fab is essentially related to the die yield, which is calculated from the ratio of the probed good dies to gross dies on the wafer. Both the line yield and die yield are important factors affecting the wafer cost, because manufacturing costs are, in general, inversely proportional to yield. Process improvement through the yield analysis is a vital part of FeRAM manufacturers.

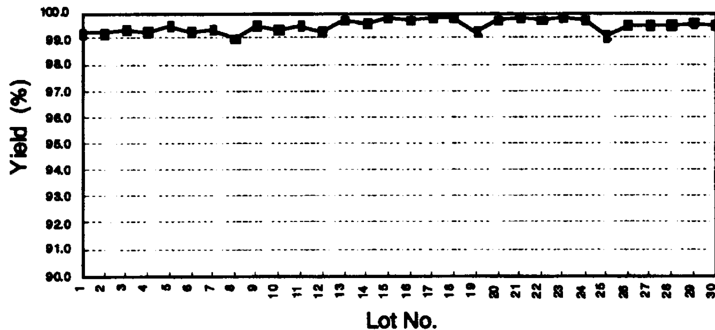

FIGURE 10 A die yield variation from lot-to-lot provided by a 0.8-μm FeRAM fab line.

Yield Analysis

In the following, we will intend to figure out some ferroelectric specific issues by making an yield analysis on a mature 0.8-μm and single-poly

FeRAM fab line. Since the line yield from the fab is approximately 100%, the yield analysis is focused on the defect density.

Figure 10 shows a die yield variation at the first functional test from lot-to-lot for the first 30 wafer lots for a logic LSI incorporating 1-kbit FeRAM. The die yield is well-saturated, and the average yield is 99.3%. The die yields from wafer-to-wafer are also scattered above 95%. Letting D_c and D_f be the defect densities for the CMOS front-end process and for ferroelectric back-end process, respectively, we can predict the die yield based on the binomial yield model:

$$Y = [1 + A(D_c + D_f)/\alpha]^{-\alpha} \quad , \qquad (1)$$

where Y is the defect-limited yield, A is the die area, and α is the cluster factor representing the gathering or clustering of the failure causing defects on a die. We used $\alpha = 2$, which is adopted as a standard value by the Semiconductor Industry Association (SIA). Let us consider a mature 0.8-μm CMOS process followed by a ferroelectric back-end process being devoted to the 1-kbit embedded LSI fabrication. Since the die area is 3.9 mm^2, the total defect density, $D_c + D_f$, is calculated to be 0.23 defects/cm^2 from Eq.(1). This defect level is as low as that in advanced CMOS front-end processes. Of course Eq.(1) can not be applied directly to the yield prediction because the embedded LSI is a composite die involving logic, FeRAM, analog, and other types of circuitry. However, this rough estimation implies that D_f in our mature fabrication line is extremely smaller than D_c.

The most frequent failure causing defects in the ferroelectric back-end process are particles generated during the MOD spin-coat, film-

growth anneal, and ferroelectric etch steps. The size of ferroelectric particles is sometimes larger than the thickness of the pre-metal dielectric (PMD) layer, so that the underlying particles cause breaks of a metal connection line on the upper layer. Figure 11 shows an anomalous defect caused by a Pt particle. These ferroelectric-specific particles can be reduced by making corrective actions on maintenance schedules of process tools.

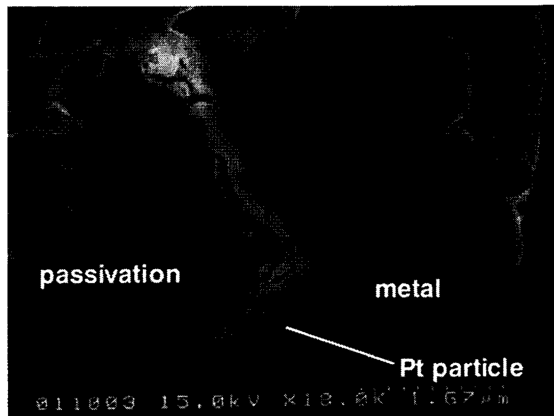

FIGURE 11 A defect caused by a Pt cluster particle resulting in an error due to short and/or open circuit.

PROCUREMENT OF RELIABILITY

The data retention ability is strongly dependent on temperature because the ferroelectricity is sensitive to temperatures near the transition point.[20]

However, the use conditions ensure sufficiently lower temperatures than the critical point of SBTN. Therefore retention failures induced by thermal activation at use temperatures are primarily associated with motion of charge carriers distributed in the ferroelectric.[21,22] The retention failure distribution of a 288-bit FeRAM has been modeled in terms of infant failures associated with fast motion of free electrons or holes pumped out from shallow traps and random failures associated with slow motion of ionic charges.[21,23] These failure models suggest that infant failures can be screened out by applying an excess stress for a proper period of time. The temperature dependence of the retention failure rate for screened LSIs incorporating FeRAMs is shown in Fig. 12. Extrapolation of the data predicts that the failure rate of either type of FeRAM is lower than 100 FITs at use temperatures. The activation energies higher than 1 eV are similar to those for slow diffusion of ionic charges (e.g., oxygen vacancies and ionic impurities).[24] Thus the further improvement in data retention ability can be achieved by reducing the oxygen defects and ionic impurities in the ferroelectric.

Another measure for the data retention ability is radiation hardness. For use in freight identification systems, x-ray exposure is a common environmental concern for the data integrity because x-rays may generate unintended charges in FeRAMs.[22] Figure 13 shows the nonvolatile component P_{nv} of switchable polarization of 5x5 μm^2 SBTN capacitor array test structures after x-ray irradiation with a continuous x-ray source whose emission intensity is 500 R/min. The capacitors were set at 2.43 V and preserved P_{nv} was measured at the same voltage after x-ray irradiation for a selected period of time. The capacitors well withstand x-rays of up to 5000 R in intensity, which is higher than those used at boarding gates in

air terminals. A similar test was also made on 288-bit FeRAMs programmed at 2.43 V. These FeRAMs exhibited no upsets in programmed data even after x-ray irradiation.

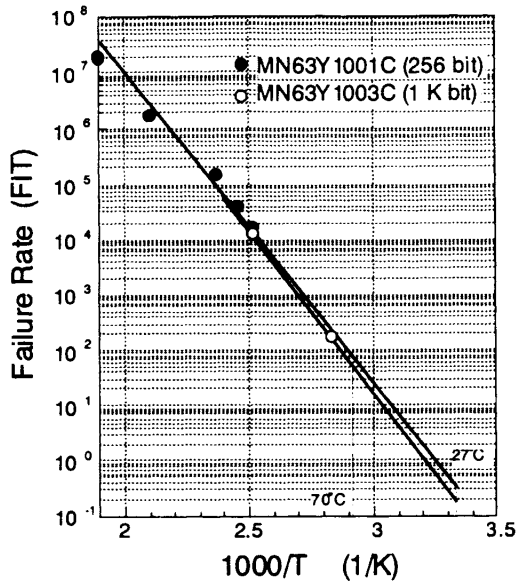

FIGURE 12 Retention failure rate *vs*. temperature for typical FeRAMs based on SBTN incorporated in LSIs.

Since the polarization is switched by applying a field between the facing electrodes of the ferroelectric capacitor, external field disturbance is a remaining concern for the data integrity of FeRAMs. Figure 14 shows P_{nv} of SBTN capacitors after radio wave irradiation for 1 s at several

frequency sweep ranges. The capacitors were programmed at 2.43 V and preserved P_{nv} was measured at the same voltage after radio wave irradiation. The incident plane in which the electric filed is oscillating was chosen to be parallel to the capacitor plates and the field strength was

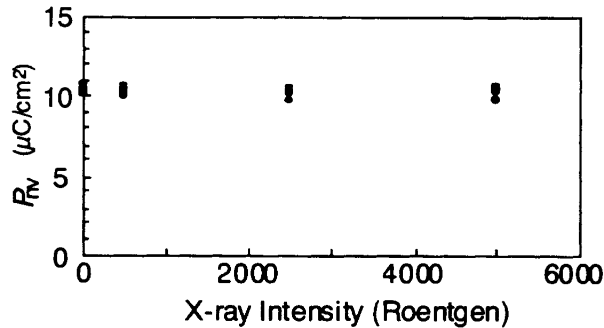

FIGURE 13 X-ray irradiation effect on P_{nv} of SBTN capacitors

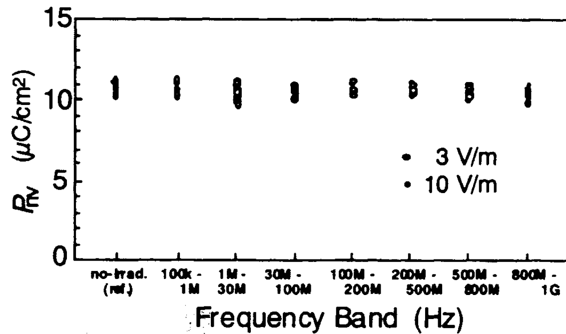

FIGURE 14 Influence of radio waves on P_{nv} of SBTN capacitors

selected to be 3 V/m and 10 V/m whose amplitudes were modulated by 80 % at 1 kHz. The data shows neither field can cause any degradation in P_{nv}. This consequence was also confirmed by subsequent irradiation tests on a lot of 288-bit FeRAM parts programmed at 2.43 V. The field disturbance resulted in no upsets in programmed data.

SUMMARY

Because of high operation speed and low power consumption of FeRAMs, contactless IC card manufacturers have started to incorporate FeRAMs into embedded LSIs. A mature 0.8-μm FeRAM with a fairly stable set of ferroelectric processes has been devoted to the fabrication of 125-kHz and 13.56-MHz logic LSIs with 288-bit and 1-kbit FeRAMs, respectively, for identification. The leading-edge 0.6-μm FeRAM technology has proven its indispensability to embedded LSIs for electronic commerce. The reliability data including the radiation influence have proven the potential capability of FeRAMs in embedded LSIs for the present contactless IC card applications. The remaining challenges toward systems-on-chips with mega-bit FeRAMs for IC cards include the following: reconfigurable logic technology, stacked cell integration, damage-less processing, and high-performance materials technology. Although in the last decade bismuth-layered perovskites made a dramatic impact on the proliferation of FeRAMs, more radical ferroelectric materials withstanding high endurance cycles (> 10^{15}), high retention temperatures (> 125°C), and hydrogen-rich fine processing will be required for future nonvolatile memories in systems-on-chips. These innovative material and processing approaches will evolve FeRAMs into a major manufacturing segment of

semiconductor industry in the upcoming 21st century.

Acknowledgments

The authors thank Dr. C. A. Paz de Araujo and the staff of Symetrix Corporation for valuable discussions and technical support for this work. They also thank Dr. G. Kano and M. Kzumura, a senior adviser and a director of Matsushita Electronics Corporation, respectively, for their continuous encouragement.

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