

A Read-Disturb-Free Ferroelectric Gate FET Memory

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The enhancement-type ferroelectric gate field-effect transistor (FeFET) requires a read biasing voltage to the gate to secure a sufficient on/off current ratio. However, disturb (depolarization) of the ferroelectric by repetitive applications of read biasing voltage to the gate is a potential reliability concern. This paper deals with the disturb issue for an experimentally fabricated FeFET with a stacked gate comprised of metal/SrBi₂Ta₂O₉/CeO₂. A significant difference between a high ON current and a low OFF current is brought about and sustained after a large number of read operations by choosing a proper gate voltage, which is not only enough to make a positively programmed FeFET turn on, but also effective to prevent the disturb effect.

Keywords: ferroelectric memory; FET; SrBi₂(Ta,Nb)₂O₉; FeFET

INTRODUCTION

The advantage of a ferroelectric gate field-effect transistor (FeFET) is its ability to read data without alternative reversals of the polarization state. A FeFET is therefore expected to provide an unlimited number of read cycles as well as fast random access cycles, high density, low power consumption, and high endurance of rewrite cycling.^[1, 2] Except for the FeFET, none of the nonvolatile memories currently available have all the above desirable features. Thus the FeFET can be the ultimate semiconductor memory.

The fundamental gate structure of the FeFET is a series combination of a ferroelectric capacitor and a metal-insulator-semiconductor (MIS) capacitor with a floating gate in-between these two capacitors, as shown in Fig. 1. To bring about channel conduction, a certain voltage is applied to the floating gate in the case of an *n*-channel MIS transistor. Programming of the FeFET is made by pulsing the gate with a relatively high voltage. When the FeFET is pulsed with a sufficiently positive voltage, the floating gate voltage V_{FG} after programming is determined from the cross point of the programmed hysteresis loop and the load line of the MIS capacitor crossing the origin on the charge-voltage (Q - V) plane. If V_{FG} is greater than the turn-on voltage V_T of the *n*-channel MIS transistor, a conducting channel exists even with zero gate voltage applied. Therefore, a normally on FeFET is readily obtained using a high-coercive-voltage material, such as $Pb_{1-x}Zr_xTiO_3$, for the ferroelectric. When the FeFET is pulsed with a sufficiently negative voltage, the floating gate voltage after programming is also determined in the same manner described above. In such a case, V_{FG} is negative all the time as far as the polarity of the polarization is unchanged. Thus

normally on and off FeFETs with zero gate voltage applied can be made by suitable choice of materials and programming voltages.^[2-5]

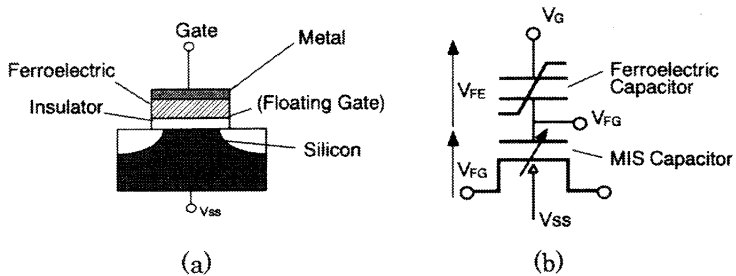


FIGURE 1 (a) A cross-sectional view of a MFIS-structured FeFET. (b) Equivalent circuit.

These types of FeFETs, however, have two major drawbacks. First, V_{FG} in the case of a positively programmed FeFET is slightly greater than V_T , so that even a small amount of leakage current results in a decrease in V_{FG} , leading to disappearance of the conducting channel. Therefore the data retention ability is dominated by the charge retentiveness of the floating gate between the ferroelectric and insulator. The second drawback is the complexity of the program/read scheme of a selected memory cell, being isolated with an additional select transistor from many other normally on FeFETs sharing the same bit-line selected, in a simple matrix array.

To solve the above drawbacks, an enhancement-type FeFET has been proposed.^[6] This type of FeFET does not conduct with zero gate voltage applied. Only a positively programmed FeFET has a conducting channel with a proper positive gate voltage applied. Thus the FeFET

can possess either ON or OFF state, depending on the polarity of the programming voltage, for a proper positive gate voltage, or a high-impedance state with zero gate voltage applied, which allows a simple cell architecture without a select transistor to the bit-line. Accordingly, the enhancement-type FeFET requires a proper gate voltage V_G for every read cycle to differentiate the two programmed states. However, the application of positive gate voltage not only enlarges the difference between the ON and OFF currents but also disturbs the polarization of a negatively programmed FeFET, because the positive gate voltage causes a reverse bias to the negatively poled polarization even if the positive gate voltage is sufficiently lower than the programming voltage. For a positively programmed FeFET, in addition, a reverse bias to the polarization also appears when the gate is grounded after reading. As the read operation is repeated, therefore, the polarizations of both positively and negatively programmed FeFETs may decrease gradually, tracing on minor hysteresis loops, and eventually collapse. Thus read disturb is a potential reliability concern for the operation of enhancement-type FeFETs.

In this paper we analyze the operation of an enhancement-type FeFET with a metal/SrBi₂Ta₂O₉/CeO₂ gate structure whose MIS transistor under the stacked ferroelectric capacitor turns on only when the FeFET is programmed positively and the floating gate is made positive for read. We also consider optimal conditions for programming and read operations to bring about a sufficient difference between the ON and OFF currents to suppress read disturb of the FeFET.

OPERATION OF THREE-STATE FeFET

If the FeFET parameters, the ferroelectric capacitance, the MIS capacitance, and the programming voltage, are chosen properly, both values of V_{FG} corresponding to the positively and negatively programmed states, respectively, can be less than that of V_T after the programming voltage is removed from the gate. This situation can be made when the hysteresis loop of the ferroelectric given under an adequate programming voltage is not saturated, as shown in Fig. 2(a), because the voltage across the ferroelectric is a fraction of the gate voltage applied, which is mostly insufficient to saturate the polarization.^[7] Then the points at which the load-line of the MIS capacitor crosses the minor hysteresis loop provide different values of V_{FG} after programming, corresponding to the positively and negatively programmed states. If the ferroelectric capacitor is poled along a small minor hysteresis with a positive programming voltage, as shown in Fig. 2(b), V_{FG} after programming is made positive, which is less than V_T . If

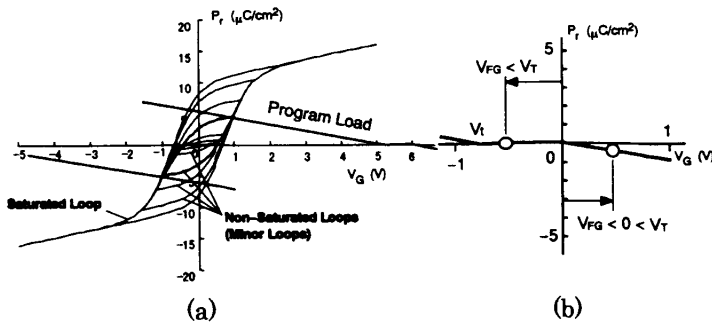


FIGURE 2 Operation of a three-state FeFET programmed using a non-saturated minor hysteresis loop.

the ferroelectric capacitor is poled along the small minor hysteresis with a negative programming voltage, as shown in Fig. 2(b), V_{FG} after programming is made negative, which is also less than V_T . Hence the FeFET has no conducting channel when the programming voltage is removed from the gate.

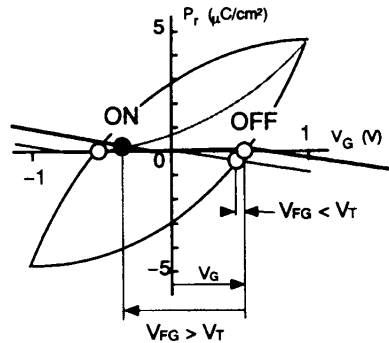


FIGURE 3 Read operation of a three-state FeFET with a slightly positive gate voltage.

The value of V_G for read is chosen to make V_{FG} greater than V_T for a positively programmed FeFET and less than V_T for a negatively programmed FeFET, so that only the positively programmed FeFET turns on. This value of V_{FG} is determined by the crossing of the minor hysteresis with the load-line of the MIS capacitor shifted by the value of V_G along the voltage axis, as shown in Fig. 3. If the slope of the load-line is small with respect to the ramp-up of the hysteresis curve, V_{FG} for a positively programmed FeFET readily exceeds V_T by making V_G positive even slightly. Accordingly, the positively programmed

FeFET turns on even if V_G is less than V_T . In addition, V_{FG} of a negatively programmed FeFET for a small value of V_G is approximately zero, so that the negatively programmed FeFET does not turn on. Thus small values of V_G less than that of V_T are enough to modulate the channel conductance of the MIS transistor. The states of the FeFET modulated by the gate voltage are summarized in Table 1.

TABLE 1 Read operation of a three-state FeFET with a slightly positive gate voltage.

Read V_G (V)	Program	
	positive	negative
0	OFF	OFF
$0 < V_G < V_T$	ON	OFF

FeFET CHARACTERIZATION

The fabricated FeFET has a stacked Pt/SrBi₂Ta₂O₉/CeO₂ gate structure on a *p*-type silicon substrate. A SrBi₂Ta₂O₉ film of 190nm in thickness and a CeO₂ film of 20 nm in thickness were directly grown on the substrate using a metal-organic decomposition technique.^[8] There is also a native oxide layer of about 5 nm in thickness between the CeO₂ film and the silicon substrate. The photolithographic dimensions of the gate are 16 μm in width and 8 μm in length.

The drain-source current I_{DS} versus V_G characteristics are given in Fig. 4 for programming voltages of ± 8 V and a drain-source voltage of 0.6 V. After programming, both the positively and negatively

programmed FeFETs exhibit a low ON current at $V_G = 0$ V. As V_G is increased, I_{DS} of the positively programmed FeFET ramps up rapidly, whereas I_{DS} of the negatively programmed FeFET remains constant for up to $V_G = 1$ V, at which the onset of switching from the low OFF current state to the high ON current state appears. The difference between the high ON current and the low OFF current is maximized at $V_G = 1$ V. Even for $V_G = 0.6$ V, however, a sufficient on/off current ratio greater than 10^2 is obtained.

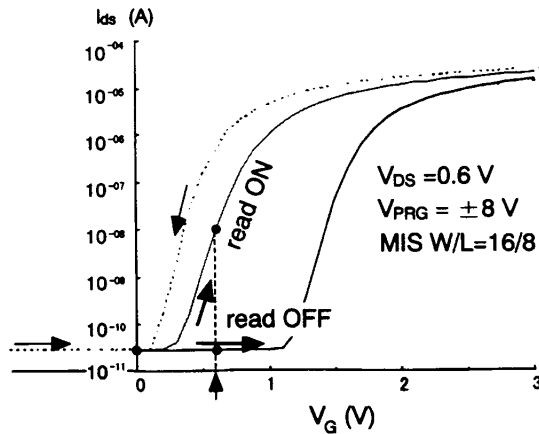


FIGURE 4 $I_{DS} - V_G$ characteristics of a three-state FeFET.

DISTURB EFFECT

Variations in I_{DS} with the number of pulses of $V_G = 0.6$ V are shown in Fig. 5. The drain-source voltage is 0.6 V. The high ON current

decreases for the first 10 pulses and subsequently remains constant for more than 10^3 pulses. The low OFF current, on the other hand, is almost constant for more than 10^3 pulses. The FeFETs are therefore free from read disturb when V_G is as low as 0.6 V, whereas this voltage is enough to make the positively programmed FeFET turn on. These results indicate that the biased polarization cycled under very weak fields does not vanish even with a large number of repetitive read operations.

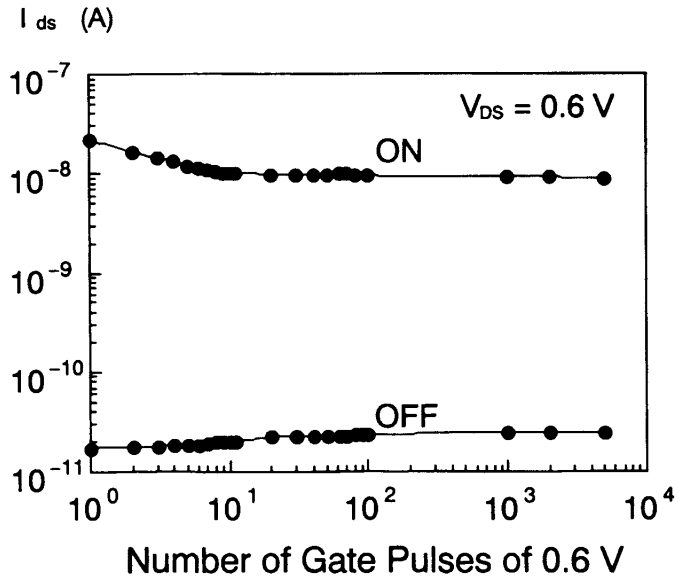


FIGURE 5 Drain-source current vs. number of gate pulses of $V_G = 0.6$ V for a three-state FeFET.

SUMMARY

The operation of an enhancement-type FeFET was analyzed. It was shown that the FeFET has no conducting channel after programming when the FeFET is programmed using a small minor hysteresis loop. We also estimated that small values of the gate voltage less, than that of the turn-on voltage of the MIS transistor underlying the stacked ferroelectric capacitor, are enough to modulate the channel conductance of the MIS transistor. A significant difference between a high ON current and a low OFF current was brought about and sustained after a large number of read operations by choosing a proper gate voltage, which is not only enough to make a positively programmed FeFET turn on but also effective to prevent the disturb effect.

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