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High Density and Long Retention Non-Destructive Readout FeRAM Using a Linked Cell Architecture

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A 64 Kbit non-destructive readout (NDRO) ferroelectric random access memory (FeRAM) using a 0.6-μm technology is described. The NDRO FeRAM uses a novel linked cell architecture, which minimizes the circuit overhead accepted in Flash memories. This test device has shown 10-year retention and unlimited read operation. An 120-ns NDRO operation is performed at a read voltage of 2.2V. Circuit techniques used in the NDRO FeRAM include: (1) direct programming of ferroelectric capacitors, (2) automatic restoring of read data, and (3) data storing under zero bias conditions. The unique linked cell architecture allows for scaling a cell size down to $6F^2$, where F is the minimum feature size available.

Keywords: ferroelectric memory, non-destructive readout, FET, FeRAM

INTRODUCTION

Ferroelectric gate field-effect transistors (FeFETs) have a potential ability to read stored data without alternative switching of polarization and therefore non-destructive readout is achieved leading to an unlimited number of read cycles [1,2]. The FeFET with a simple metal-ferroelectric-metal-insulator-silicon (MFMIS) or metal-ferroelectric-insulator-silicon (MFIS) gate structure, however, is certainly plagued with premature data retention life (~10^6 s), *i.e.*, the floating gate voltage decreases in a short time as the preserved charge on the floating gate leaks out though the ferroelectric when the device is powered off [3,4]. In the case of DRAM-like cell structures such as a two-transistor-two-capacitor (*2T/2C*) cell currently used in existing FeRAMs, in contrast, the data retention characteristic is good enough for practical use because the programmed polarization is preserved at zero bias voltage across the ferroelectric capacitor. This stable condition secures a long retention life, for instance, for more than 10 years [5]. However, reading data from this type of memory cell requires polarization switching to extract the preserved charge. Thus, the memory cell needs a subsequent rewrite operation in order to restore the switched polarization. Consequently, the polarization is cycled every reading, which causes fatigue of the ferroelectric before reaching a specified number of read cycles, greater than 10^{15}, required for universal memory applications.

In this paper, we demonstrate a non-destructive readout (NDRO) operation using a 64 Kbit FeRAM test vehicle, which can offer 10-year retention and an unlimited number of read cycles. Some innovative circuit techniques used for achieving the NDRO operation are described. The minimal cell size achievable using a one-transistor-one-capacitor (1*T*/1*C*) stacked cell structure with a linked cell architecture is also estimated.

OPERATION PRINCIPLES OF NDRO FeRAM

Long Retention Programming

Figure 1 shows a circuit of the unit cell for the NDRO FeRAM, which is a series combination of a ferroelectric capacitor C_F and a transistor Q_1. In this configuration, a "1" is programmed into C_F by pulsing the SET line to the supply voltage, V_{DD}, to switch the polarization into the upper remanent polarization state, which is indicated by the upper intercept of the *Q-V* hysteresis loop on the *Q*-axis in Fig. 2. Meanwhile, the reset transistor Q_2 is turned "on" and the select transistor Q_3 is turned "off". A "0" is assigned to the opposed remanent polarization state. This state can be established by pulsing the RST line to V_{DD} with turning Q_2 "on" and Q_3 "off". After programming, Q_3 is turned "on" in order to preserve the programmed remanent polarization under the condition of zero bias voltage, which is essentially the same situation as in existing *2T/2C* memory cells during power-off. It is therefore expected that this memory cell can preserve the data for a long time.

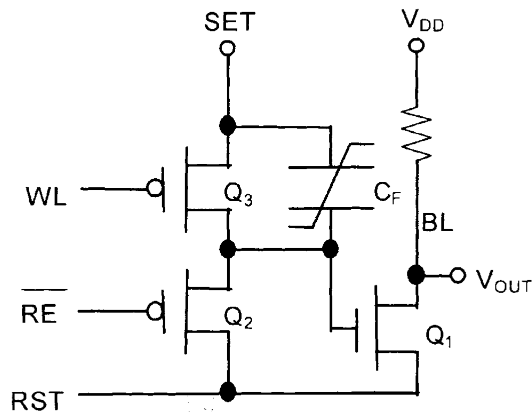

FIGURE 1 Circuit implementation of a non-destructive readout memory cell.

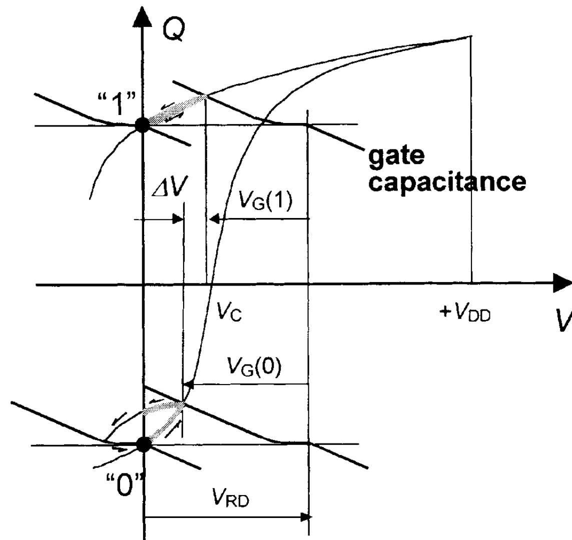

FIGURE 2 A portion of a Q-V hysteresis loop overlaid with load-lines of a gate capacitance of a transistor for reading.

Non-Destructive Readout

After programming, there is no difference in V_G between a "1" and a "0" at the floating gate of Q_1. In order to sense whether a "1" or a "0" has been stored, a positive read bias voltage V_{RD} is applied to the SET line. Then V_{RD} is divided into a voltage V_F across C_F and a voltage V_G across the gate of Q_1. Since the gate capacitance of Q_1 is generally smaller than the capacitance of C_F, a large portion of V_{RD} is sustained by V_G. As a result, V_F can be less than the coercive voltage V_C of the ferroelectric capacitor. Therefore, the polarization for the "0" is never switched into the opposite state at such a voltage of V_{RD} ($V_F < V_C$).

However, V_{RD} can bring about a definite voltage on the gate of Q_1 depending on the swing of polarization for either the "1" and the "0". Since the swing of polarization for the "0" is steeper than that for the "1", V_G for the "0" is greater than that for the "1", as shown in Fig. 2. This leads to a higher channel conductance of Q_1 for the "0" than that for the "1". Consequently, the clamped voltage V_{OUT} appears at the drain node of Q_1 in accordance with the stored data either the "0" or the "1".

Restoring of Read Data

When V_{RD} is applied to the SET line, the polarization for the "1" moves along the upper curve of the programmed hysteresis loop, as shown in Fig. 2. When V_{RD} is removed, the polarization for the "1" returns to the initial position on the Q-axis. On the other hand, a read disturb problem may occur for reading the "0", because the remanent polarization for the "0" is oppositely directed against V_{RD}. When V_{RD} is removed, the position of the polarization steps up from its original one on the Q-axis. Therefore, repetitive read operations may cause a gradual decrease in remanent polarization until the polarization is vanished. Fortunately, the read disturb for the "0" can be diminished by switching the polarization back immediately after reading. This can be made by grounding the SET line before grounding the floating gate to give rise to a reverse bias voltage across the ferroelectric capacitor. The small gate capacitance of Q_1 can bring about such an effective reverse bias voltage to restore the deviated polarization. Finally, turning Q_2 "on" with the means to remove the reverse bias completes this restoring process. Therefore the deviated polarization is restored automatically and therefore read disturb is not possible in this memory cell. Since the memory cell does not have a restoring delay, the cycle time can be shortened.

Read-Disturb-Free Operation

Test unit cells for NDRO were fabricated using 0.6-μm technology and the ferroelectric capacitors were programmed by applying V_{DD} to the SET or RST line, according to the data either "1" or "0". Characteristics of read disturb at V_{RD} = 2V is shown in Fig. 3. The unit cells exhibit sufficient margin for up to 10^{12} cycles, which indicates that the read disturb effect is diminished effectively by restoring the flipped polarization utilizing a reverse bias voltage generated at the floating gate. During the read operation, the maximum field across C_F for V_{RD} = 2 V is approximately 34 kV/cm. This field is lower than the coercive field (~50 kV/cm) and also much lower than those (~200 kV/cm) used for reading in existing FeRAMs using destructive readout. According to an empirical model for the electric field acceleration of fatigue in ferroelectrics [6], the reduction in the field strength from 200 kV/cm to 34 kV/cm extends the number of endurance cycles by a factor of 10^6. Since the endurance of the destructive readout FeRAMs is specified at greater than 10^{10} cycles, the number of read cycles for these test cells are expected to exceed 10^{16} cycles.

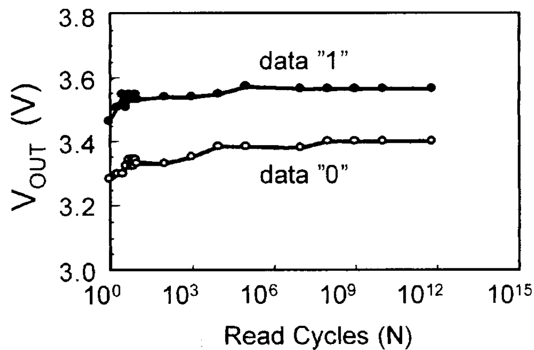

FIGURE 3 Change in V_{OUT} as a function of the number of read cycles at V_{RD} = 2 V.

HIGH-DENSITY CHALLENGE

Linked Cell Architecture

Since the unit memory cell for NDRO is comprised of one capacitor and three transistors, the reduction in cell size is a vital challenge to high-density NRDO FeRAMs. A solution for minimizing the chip penalty

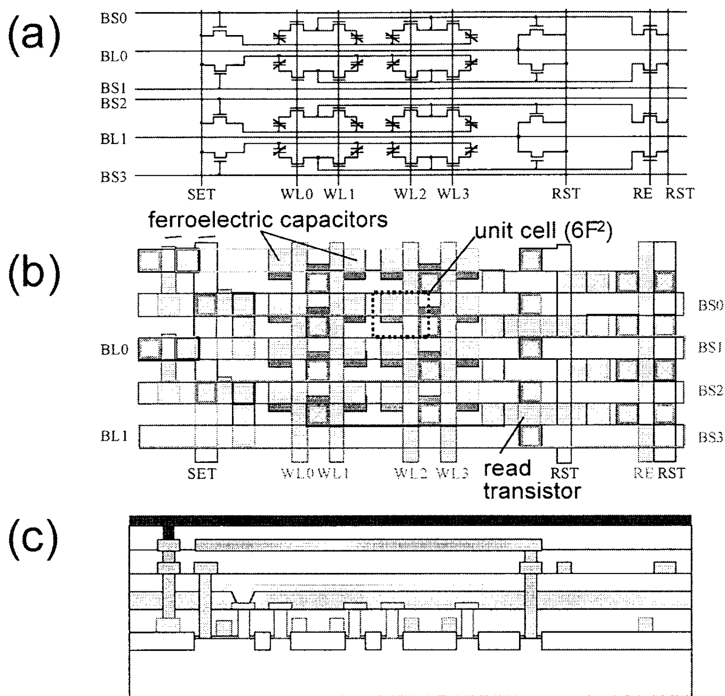

FIGURE 4 Linked cell structure with four 1T/1C cells per block arranged using the minimum pitch defined by the gate width F: (a) Circuit. (b) Layout. (c) Cross-sectional view.

is to adopt a linked cell architecture. Figure 4 shows such arrays of four $1T/1C$ linked cells per block designed in accordance with the minimum pitch F, which is defined in terms of the gate width. Although this circuit uses a folded bit line architecture, the word lines (WL0-WL3) can be shared with pairs of neighboring cells by disconnecting one of the neighboring blocks with the block select (BS) transistor from the bit line (BL) during the read operation. It shows that each cell can be placed in an area of $6F^2$, if a four-level metal technology is combined with this circuit configuration. The average cell size per bit reaches $6F^2$ with increasing the number of cells linked to a transistor for reading when a circuit overhead at the terminals of the block is considered. The authors ascertained that the NDRO memory works by 16 cells per block.

64 Kbit NDRO FeRAM

Figure 5 shows the logical organization of a 64 Kbit NDRO FeRAM using $2T/2C$ cells fabricated for experiment. Since a 0.6 μm and planer cell technology was used, the area of the $2T/2C$ cell is 110 μm^2, which is unexpectedly large but good enough for feasibility studies of the NDRO operation. The die size is 6.7 x 5.25 mm^2. The memory array is divided into 32 blocks in column, each consisting of 16 word lines, and is divided into 8 segments in row, each consisting of 16 bit line pairs. Thus the NDRO FeRAM is organized as 8 K x 8 bits, which can be programmed 1 byte at a time. Each segment has a row decoder on the left-hand side, which selects a word line and provides a routing channel for writing an input data to a selected column.

Figure 6 shows a circuit schematic and the layout used in the 64 Kbit NDRO FeRAM. In each block, 16 cells are linked in parallel and connected to the gates in pair of transistors for reading, whose drains are connected to bit line pair and the sources are connected to a pair of RST lines. A selected cell is programmed with complementary data through a

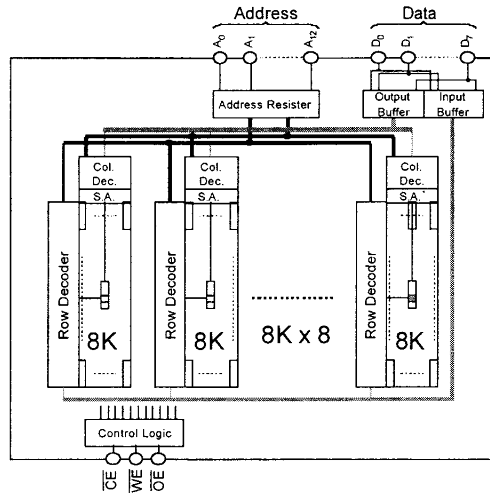

FIGURE 5 Block diagram of a 64 Kbit NDRO FeRAM.

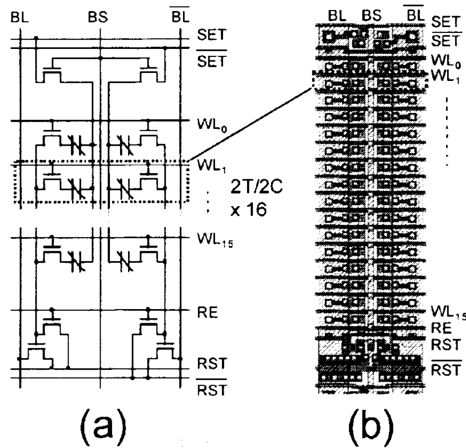

FIGURE 6 A memory cell block with 16-2*T*/2*C* cells for a 64 Kbit NDRO FeRAM. (a) Circuit. (b) Layout.

pair of SET lines located at the top of the block and the pair of the RST lines located at the bottom of the block. The read bias voltage V_{RD} is also provided through the SET line pairs. A voltage difference appearing across the pair of bit lines comes in a sense amplifier selected with a column decoder to get an output, either "1" or "0", through the output buffer. Typical operation conditions for a selected 2T/2C cell are summarized in Table I.

TABLE 1 Operation conditions for a 2*T*/2*C* linked cell.

	BS	WLn	RE	SET	$\overline{\text{SET}}$	RST	$\overline{\text{RST}}$
Read	5V	5V	0V	2V	2V	0V	0V
Write "1"	5V	5V	5V	5V	0V	0V	5V
Write "0"	5V	5V	5V	0V	5V	5V	0V

CHIP PERFOREMANCE

Figure 7 shows simulation results for the bit line voltages after the SET lines are pulsed for reading at different temperatures. A typical SET line voltage for reading is 2.2 V, which provides a bias voltage of 0.6 V across the selected ferroelectric capacitor. This value is less than the coercive voltage, thereby leading to a NDRO operation. A sufficient difference in the signal level between a "1" and a "0" appears within a 20-ns delay from the leading edge of the V_{RD} signal. When the bit line reaches a threshold voltage for initiating the operation of a sense amplifier. The delay by the time that the data are available at the output buffer is 50 ns even at 95°C. There is no restoring cycle afterward.

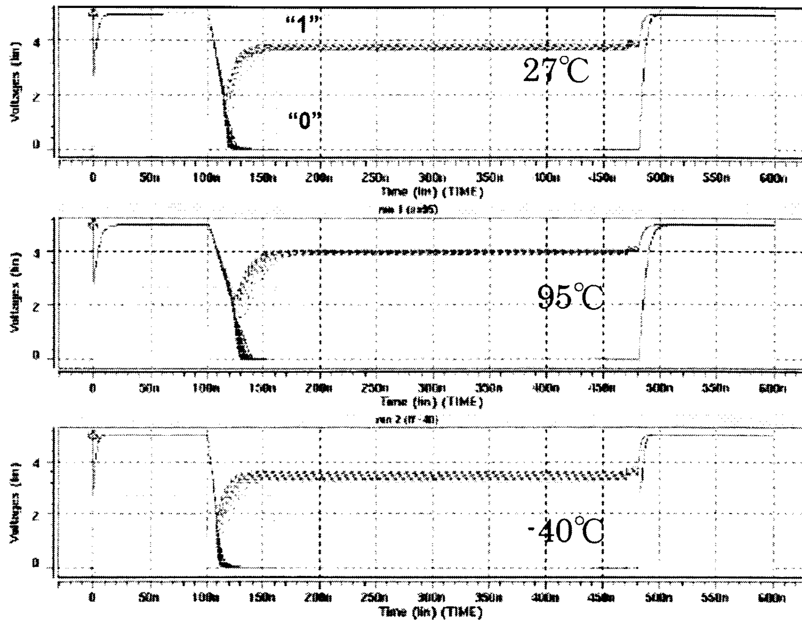

FIGURE 7 Waveforms of the bit line voltages for read operations at different temperatures.

An access shmoo plot for the 64 Kbit NDRO FeRAM is shown in Fig. 8. The lower operation limit in V_{DD} is 4 V. Yet an access time of 120 ns was achieved at V_{DD} = 5 V. The operation voltage for the NDRO FeRAM can be lowered to below 2.2 V by further reduction in the thickness of the ferroelectric capacitor.

A photograph of the 64 Kbit NDRO FeRAM is shown in Fig. 9.

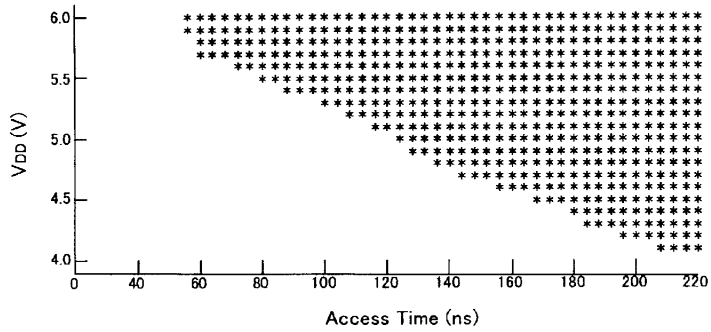

FIGURE 8 Access shmoo plot.

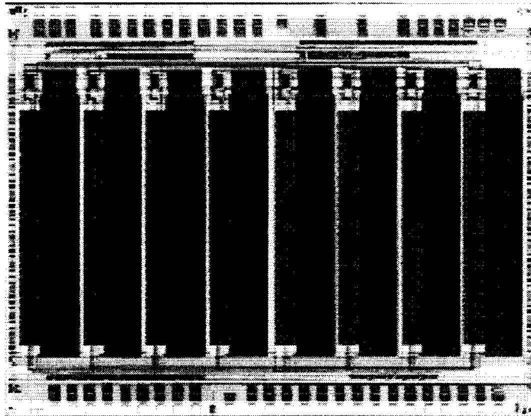

FIGURE 9 Photo of a 0.6-μm 64 Kbit NDRO FeRAM.

SUMMARY

A non-destructive read-out (NDRO) ferroelectric memory (FeRAM) has achieved long retention and disturb-free readout characteristics. It features a direct programming scheme of ferroelectric capacitors, automatic restoring of read data after reading for read-disturb-free performance, and data storing under zero bias conditions for longer retention characteristics. A 64 Kbit NDRO FeRAM fabricated using a 0.6-μm technology has 120-ns access time at a read voltage of 2.2 V and proved that the linked cell architecture is an attractive choice for higher density stacked cell arrays. The minimal cell size achievable using a stacked cell structure with the linked cell architecture is expected to be $6F^2$. The simplicity, reliability, and the full process compatibility of the linked cell architecture make this approach very realistic for higher density NDRO FeRAMs.

Acknowledgments

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