IEICE TRANS. ELECTRON., VOL. E77-C, NO. 3 MARCH 1994

PAPER Special Issue on Quarter Micron Si Device and Process Technologies

Application of Ferroelectric Thin Films to Si Devices

Koji ARITA†, Eiji FUJII†, Yasuhiro SHIMADA†, Yasuhiro UEMOTO†, Masamichi AZUMA†, Shinichiro HAYASHI†, Toru NASU†, Atsuo INOUE†, Akihiro MATSUDA†, Yoshihisa NAGANO†, Shin-ichi KATSU†, Tatsuo OTSUKI†, Gota KANO†, *Members*, Larry D. McMILLAN†† *and* Carlos A. Paz de ARAUJO†††, *Nonmembers*

SUMMARY Characterization of silicon devices incorporating the capacitor which uses ferroelectric thin films as capacitor dielectrics is presented. As cases in point, a DRAM cell capacitor and an analog/digital silicon IC using the thin film of barium strontium titanate ($Ba_{1-x}Sr_xTiO_3$) are examined. Production and characterization of the ferroelectric thin films are also described, focusing on a Metal Organic Deposition technique and liquid source CVD.

key words: *semiconductor materials and devices, materials, integrated electronics, recording and memory technologies*

1. Introduction

Research and development on Si process and device technology have played an important role of the progress of ULSIs and the expansion of semiconductor industry. Taking a memory for example, recent technology evolution has enabled us to realize 256 Mb DRAM. Surpassing 256 Mb DRAM, however, a lot of complicated processing steps due to the DRAM cell structure will lead us to the decrease in production yield and the increase in cost unless new technology is introduced.

Use of ferroelectric material has been attracted attention as a major breakthrough in DRAM technology, with which 1 Gb DRAM is considered to come out from a laboratory by the end of this century [1]. In addition to the application for high-density DRAM cell capacitors, efforts for the exploitation of ferroelectric thin films have been extended to nonvolatile memories [2], metal-ferroelectric-semiconductor devices [3], and integrated bypass capacitors [4], utilizing the features of ferroelectric thin films.

This paper presents our results of production and characterization of ferroelectric thin films, especially the thin film of barium strontium titanate ($Ba_{1-x}Sr_xTiO_3$, hereafter BST), and the characterization of Si devices on which BST capacitors are formed [5]. It should be mentioned that throughout this paper the term "ferroelectric" is used for describing these films even though the hysteresis characteristics provided by spontaneous polarization are not utilized in our devices described later.

2. Preparation of Ferroelectric Thin Films

2. 1 Metal Organic Deposition

There are several ways of depositing ferroelectric thin films [6]: sputtering, spin-coating, laser ablation, CVD, etc. All of these methods are now evolving technologically and finding applications in such a wide range of disciplines that it is quite difficult to accurately compare the merits of each system.

At present we employ the conventional spin-on technique, which is called Metal Organic Deposition (hereafter MOD) technique [7], using a mixture of metal alkoxides corresponding to the required ferroelectric thin films. In this deposition process, spin-coating, drying, and sintering are involved, respectively. A photo-resist spinner is usually used for the spin-coating, which promises the lower deposition cost. The drying process affords the decomposition of residual organics, while the sintering process is carried out for crystallization of the films.

With this technique, strict stoichiometric control of the thin films can be obtained by using a homogeneous mixture of metal alkoxides, each of which has a precisely controlled composition of an individual metal. Currently we make use of newly developed alcohol-based precursors, since the stability of the organometallic compounds has a crucial effect on the spin-coating process and the drying process (i.e. the thermal decomposition process) [8].

The dependence of the lattice constant of the fabricated our BST film on the composition of Sr are

Manuscript received August 20, 1993.
Manuscript revised November 15, 1993.

† The authors are with the Electronics Research Laboratory, Matsushita Electronics Corporation, Takatsuki-shi, 569 Japan.
†† The author is with the Symetrix Corporation, 5055 Mark Dabling Blvd. # 100, Colorado Springs, CO 80918, USA.
††† The author is with the Microelectronics Research Laboratory, University of Colorado at Colorado Springs, 1420 Austin Bluffs Parkway P. O. Box 7150, Colorado Springs, CO 80933-7150, USA and with the Symetrix Corporation.

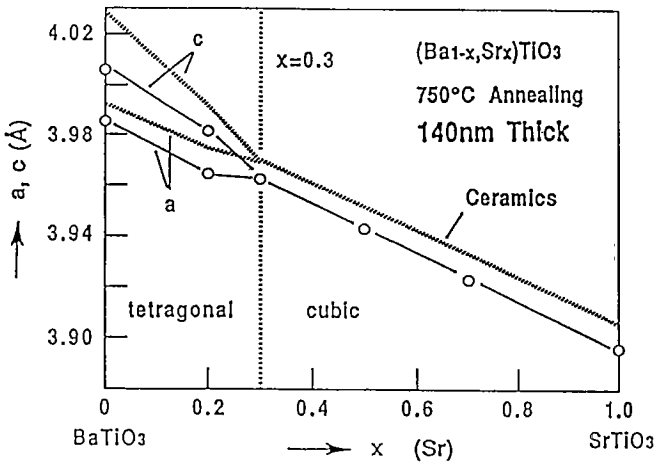


Fig. 1 Lattice constant of $Ba_{1-x}Sr_xTiO_3$ film as a function of Sr composition: (——) Thin film. (------) Bulk ceramics [10].

shown in Fig. 1 [9], where the film is deposited on Pt/Ti electrode and annealed in O_2 at 1023 K for an hour. It should be noted that the lattice constant changes in almost the same manner as bulk ceramics [10] shown in Fig. 1. Increasing the Sr content of BST, the phase transition of BST from tetragonal to cubic occurs at the Sr composition of 0.3, where the dielectric constant takes the maximum value as large as 500, which is almost the same as the bulk ceramics, too [10]. These results suggest that the BST film grown by this MOD technique has similar quality as the bulk ceramics in terms of crystallographic and electrical characteristics [9].

2. 2 Liquid Source CVD

CVD, especially MOCVD [6] is well-known as a suitable deposition technique for good step coverage, which is needed for future DRAMs. On the other hand, these reported MOCVD processes require several chemical sources and complicated control for their mixture synthesis.

Liquid source CVD (hereafter LSCVD) is a notable thin film deposition technique, which is a combination of some of the advantages of CVD and the convenience of MOD [11], [12]. It may be inappropriate to include LSCVD in the family of CVD methods because the source materials, reaction temperatures, etc. are considerably different than what are normally accepted as standard CVD conditions.

Figure 2 shows the schematic setup of LSCVD machine. A mist of stoichiometrically correct compound liquid sources, which is generated by an atomizer manifold, is injected into a vacuum chamber, together with an inert carrier gas, and the mist is distributed evenly over a rotating substrate inside the chamber. After that, a drying step is used to evaporate the organic compounds, and high temperature furnace

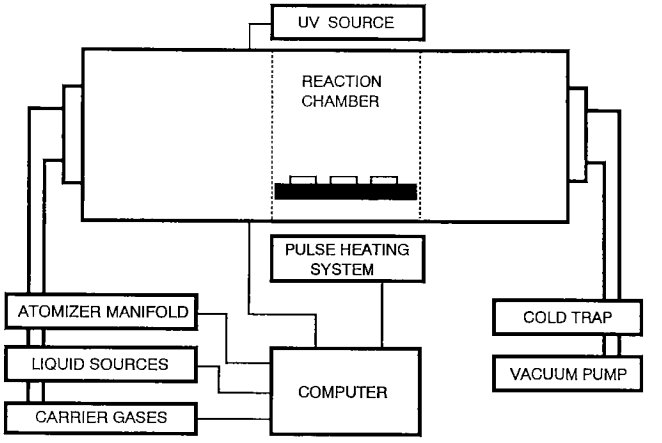


Fig. 2 LSCVD machine concept.

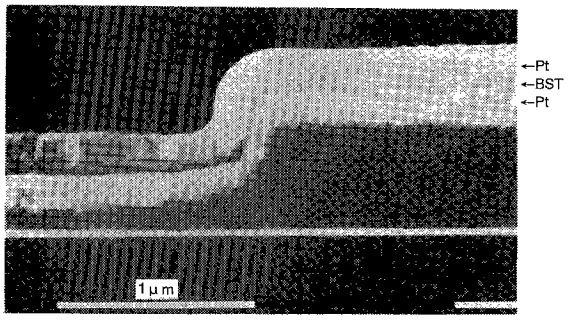


Fig. 3 Step coverage of LSCVD deposited BST.

annealing is required to crystallize the films.

This technique achieves the film cleanliness of vacuum depositions, high flexibility in controlling the film stoichiometry by changing the composition of liquid sources, and adequate step coverage shown in Fig. 3, which is the result of depositing a 50 nm film of BST on Pt by LSCVD. Figure 3 also shows the capability of preparing a ferroelectric thin film having a thickness of less than 50 nm, which will be required for gigabit DRAMs. These advantages strongly suggest the usefulness of LSCVD for future ULSI DRAMs.

3. Ferroelectric Capacitor for Integrated Circuit Devices

3. 1 The DRAM Cell

As mentioned above, complicated three dimensional cell structures have been incorporated into ULSI DRAMs in order to keep sufficient storage capacitance in the small memory cell area [13]. By using a ferroelectric thin film as a dielectric of the DRAM cell capacitor, simple cell structure can be expected to be useful for the ULSI DRAMs, even for 1 Gb DRAM.

For example, the cross-sectional view of the BST DRAM cell is shown in Fig. 4. Use of the BST film

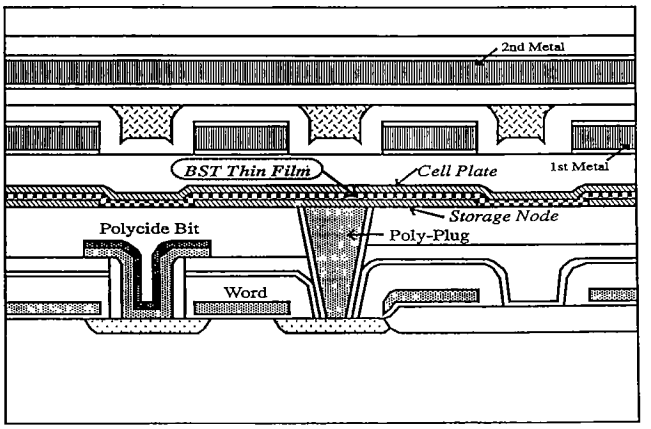


Fig. 4 Schematic cross-sectional view of planar-type single stacked cell structure.

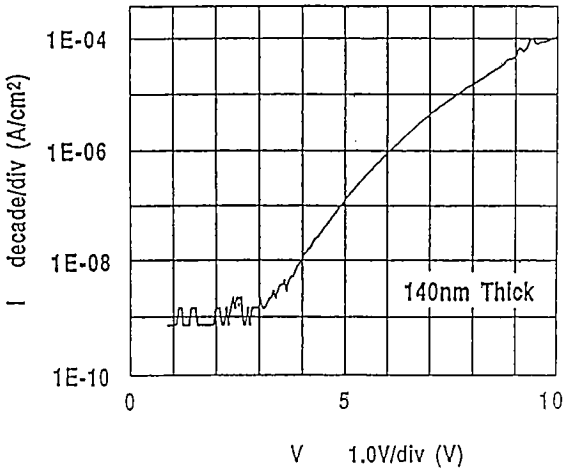


Fig. 5 Leakage current characteristics of the BST cell capacitor.

with high-dielectric constant allows to incorporate the planar-type single stacked structure into the ULSI DRAM storage capacitor. The buried polysilicon plug between silicon substrate and storage node is also used for keeping the planar-type structure.

The DRAM cell capacitor has been fabricated using the $Ba_{0.7}Sr_{0.3}TiO_3$ film as the capacitor dielectric and the Pt/TiN/Ti electrode as the storage node. The thickness of the $Ba_{0.7}Sr_{0.3}TiO_3$ film prepared by the MOD technique was 140 nm, which means the equivalent SiO_2 thickness is as thin as 1.3 nm. It is generally recognized that very thin films (e.g. the BST film which is on the order of 0.1 nm in equivalent SiO_2 thickness) is demanded for 1 Gb DRAM and beyond, which will be realized by the further development of film deposition technique, such as LSCVD [11], [12].

The leakage current characteristics of the fabricated cell capacitor are shown in Fig. 5. The leakage current is decreased down to 2×10^{-9} A/cm^2 under a supply voltage of 3.3 V, which is low enough to realize the low-power and the high-density DRAMs. The

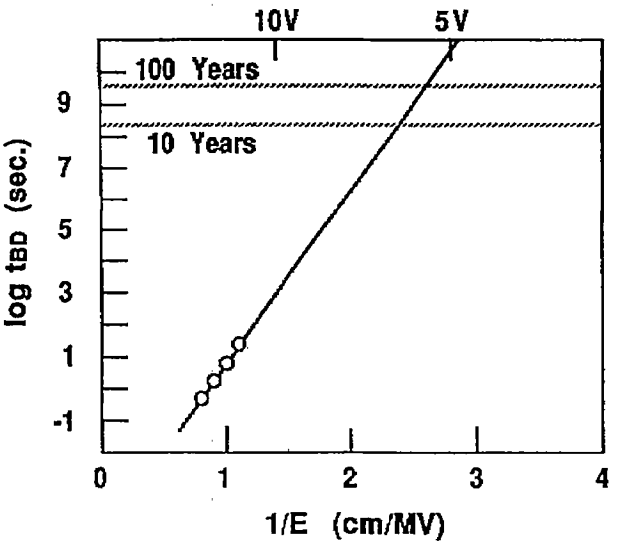


Fig. 6 TDDB characteristics of the BST cell capacitor.

TDDB (Time Dependent Dielectric Breakdown) characteristics of the fabricated cell capacitor are shown in Fig. 6. The lifetime to breakdown of the cell capacitor is concluded to be over 100 years even under a stress voltage of 5 V. These preliminary results indicate the potential of the ferroelectric thin films for the DRAM cell capacitor.

3.2 The Integrated Bypass Capacitor

Bypass capacitors are usually mounted on printed circuit boards with Si/GaAs ICs. If the bypass capacitor, which must have a large capacitance on the order of hundreds pF, can be formed inside an IC chip of normal size, the supply voltage will be effectively stabilized, resulting in the reduction of electric noise. Reduction of external pins of the IC package and flexibility of the layout of the printed circuit boards will be also expected. Ferroelectric bypass capacitors can be formed in the normal IC chip, though the conventional semiconductor technology requires a large area for fabricating bypass capacitors due to the small dielectric constants of the dielectrics used (i.e. SiN or SiO_2) [4].

In order to investigate the effects of integrated bypass capacitor, we have experimentally fabricated an analog/digital Si IC which integrates about 3800 transistors, and a ferroelectric capacitor whose dielectric was $Ba_{0.7}Sr_{0.3}TiO_3$. Figure 7 shows the top view of the IC chip, where the BST bypass capacitor is placed in the left side of the chip. The capacitance of this integrated BST capacitor was 1400 pF. The analog/digital Si IC with a SiO_2 bypass capacitor instead of the BST bypass capacitor was also fabricated as a reference.

Comparing the waveforms of the supply voltages shown in Figs. 8(a) and 8(b), high-frequency electric

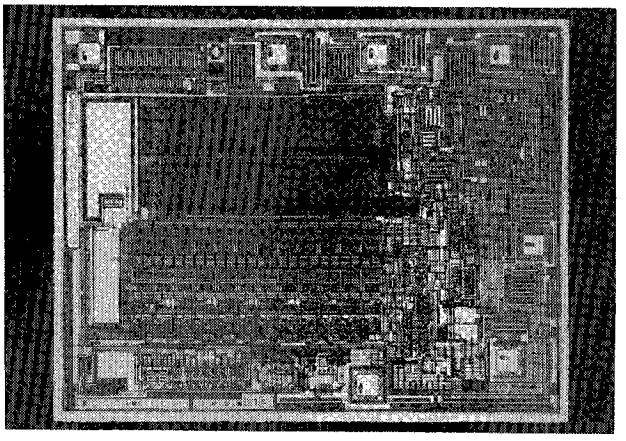
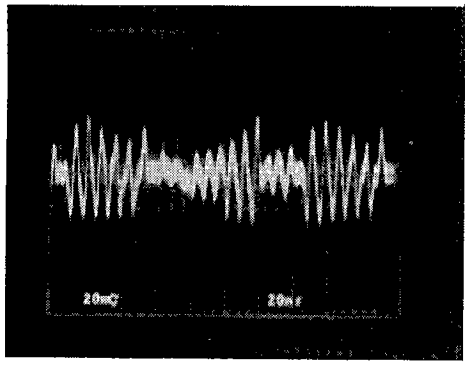
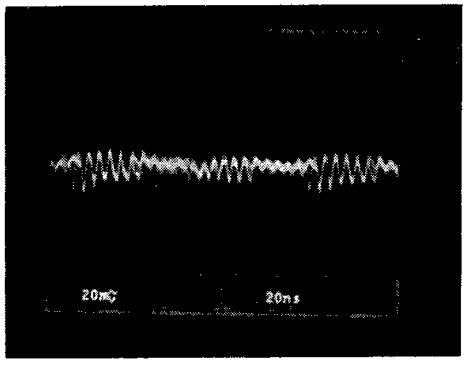


Fig. 7 Micrograph of the analog/digital Si IC chip. The chip is 1.8×2.3 mm^2.



(a)



(b)

Fig. 8 (a) The waveform of the supply voltage of the analog/digital Si IC with the 40 pF SiO_2 bypass capacitor. (b) The waveform of the supply voltage of the analog/digital Si IC with the 1400 pF integrated BST bypass capacitor.

noises (i.e. fluctuation of the supply voltage) seems to be dramatically decreased when the integrated BST bypass capacitor is used. With the frequency analysis, decrease of 70% in the amplitude of noises was found in the case of the IC with the BST capacitor, in comparison with the IC with the 40 pF SiO_2 capacitor. This suggests that the BST bypass capacitor effectively works as a high-frequency noise suppression filter. The electrical characteristics of this BST bypass capacitor, such as leakage current, TDDB, etc., are considered to be on a level with those of the BST DRAM cell capacitor described earlier, which will ensure the reliability of the bypass capacitor.

4. Conclusion

The validity of integrating ferroelectric thin films on Si devices has been presented. Use of the ferroelectric thin film for the DRAM cell capacitor is expected to be the promising way of realizing the ULSI DRAMs, especially beyond 1 Gb DRAM [1]. Concerning the integrated bypass capacitors, this idea will be widely accepted in order to suppress the electric noise from signal processors, which now becomes serious concern among digital equipment. It should be noted that the above-mentioned devices utilize high-dielectric nature of ferroelectric thin films.

In addition, application of the hysteresis characteristics of the ferroelectric thin films has been attracted attention for creating various semiconductor devices such as nonvolatile memories (ferroelectric memories), which will replace present memory devices in the future [2]. This also indicates the validity of using these films in semiconductor devices.

In conclusion, ferroelectric thin film process/device technology will play a leading role in ULSI technologies in the future, in connection with the quarter micron Si process and device technology.

Acknowledgments

The authors would like to thank Mr. H. Iwasa and Dr. T. Kawasaki for their advice and encouragement during this work, Professor J. F. Scott of University of Colorado for fruitful discussion, and Mr. N. Suzuoka for cooperation in the development of the analog/digital Si IC with the integrated BST capacitor.

References

[1] Komiya, H., "Future technological and economic prospects for VLSI," in *ISSCC Digest of Technical Papers* (San Francisco, California), pp. 16-19, Feb. 1993.

[2] Scott, J. F. and Paz de Araujo, C. A., "Ferroelectric memories," *Science*, vol. 246, pp. 1400-1405, 1989.

[3] Sinharoy, S., Buhay, H., Lampe, D. R., and Francombe, M. H., "$BaMgF_4$ thin film development and processing for ferroelectric FETs," in *Proc. 4th Int. Symp. Integr. Ferroelectrics* (Monterey, California), pp. 290-297, Mar. 1992 and references therein.

[4] Nagata, S., Ueda, T., Noma, A., Koizumi, H., Kanazawa, K., Ishida, H., Ueda, T., Tanaka, T., Ueda, D., Kazumura, M., Kano, G. and Paz de Araujo, C. A., "A GaAs MMIC chip-set for mobile communications using on-chip ferroelectric capacitors," in *ISSCC Digest of Technical Papers* (San Francisco, California), pp. 172-173, Feb.

1993.

[5] For a review of ferroelectric ceramics see Setter, N. and Colla, E. L. (ed.), *Ferroelectric Ceramics*, Birkhauser, Basel, 1993.

[6] For a review of recent progress in deposition methods of ferroelectric thin films see *Special Issue on Ferroelectric Materials and Their Applications*, *Jpn. J. Appl. Phys.*, vol. 32, part. 1, no. 9B, Sep. 1993.

[7] Mantese, J. V., Micheli, A. L., Hamdi, A. H. and Vest, R. W., "Metalorganic deposition (MOD) : a nonvaccum, spin-on, liquid-based, thin film method," *MRS Bulletin*, pp. 48-53, Oct. 1989.

[8] Tohge, N., Takahashi, S. and Minami, T., "Preparation of $PbZrO_3$-$PbTiO_3$ ferroelectric thin films by the sol-gel process," *J. Am. Ceram. Soc.*, vol. 74, no. 1, pp. 67-71, Jan. 1991.

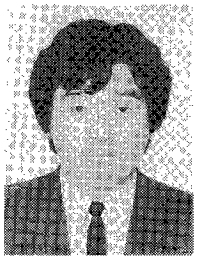
[9] Azuma, M., Scott, M., Fujii, E., Otsuki, T., Kano, G. and Paz de Araujo, C. A., "Electrical characteristics of high dielectric constant materials for integrated ferroelectrics," in *Proc. 4th Int. Symp. Integr. Ferroelectrics* (Monterey, California), pp. 109-117, Mar. 1992.

[10] Hellwege, K. -H. and Hellwege, A. M (ed.), *Landolt-Bornstein Numerical Data and Functional Relationships in Science and Technology*, vol. III/16a, Springer-Verlag, New York, 1981.

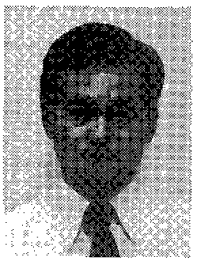
[11] McMillan, L. D., Paz de Araujo, C. A., Roberts, T., Cuchiaro, J., Scott, M. and Scott, J., "Liquid source CVD," in *Proc. 3rd Int. Symp. Integr. Ferroelectrics* (Colorado Springs, Colorado), pp. 649-657, Apr. 1991.

[12] McMillan, L. D., Roberts, T. L., Scott, M. C. and Paz de Araujo, C. A., "Deposition of $Ba_{1-x}Sr_xTiO_3$ and $SrTiO_3$ via liquid source CVD (LSCVD) for ULSI DRAMs," in *Proc. 4th Int. Symp. Integr. Ferroelectrics* (Monterey, California), pp. 666-674, Mar. 1992.

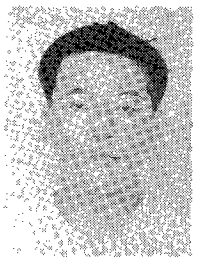
[13] Ozaki, T., Nitayama, A., Sunouchi, K., Takato, H., Takedai, S., Yagishita, A., Hieda, K. and Horiguchi, F., "A surrounding isolation-merged plate electrode (SIMPLE) cell with checkered layout for 256 Mbit DRAMs and beyond," in *IEDM Tech. Dig.* (Washington, D. C.), pp. 469-472, Dec. 1991.



Koji Arita was born in Osaka, Japan, on September 30, 1962. He received the M.S. degree in coordinated science from the University of Tokyo in 1987. From 1992 he works for Matsushita Electronics Corporation, and is currently engaged in research and development of ferroelectric devices. Mr. Arita is a member of the Chemical Society of Japan.



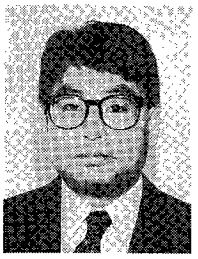
Eiji Fujii was born in Kumamoto, Japan, on March 7, 1960. He received the B.S. and M.S. degrees in applied physics from Osaka University, Osaka, Japan, in 1982 and 1984, respectively. Since joining the Electronics Research Laboratory of Matsushita Electronics Corporation, Osaka, Japan, in 1984, he has been engaged in the development of solid-state imagers, Si-TFT integrated circuits, and high-density SRAM. His current work involves the development of the integrated ferroelectric devices. Mr. Fujii is a member of the Japan Society of Applied Physics.



Yasuhiro Shimada received the B.S. degree in physical engineering from the University of Electro-Communications, Tokyo, Japan, in 1982. He joined Matsushita Electronics Corporation, Osaka, Japan, in 1982. From 1987 to 1991, he worked on R&D of excimer lasers. He is currently working for a ferroelectric device program.

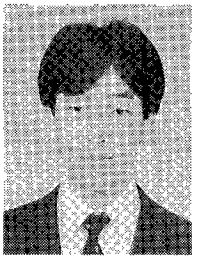
Yasuhiro Uemoto was born in Hiroshima, Japan, on January 16, 1963. He received the B.S. and M.S. degrees in electrical engineering from Kyoto University, Kyoto, Japan, in 1985 and 1987, respectively. Since joining the Electronics Research Laboratory of Matsushita Electronics Corporation, Osaka, Japan, in 1987, he has been engaged in the development of Si-TFT integrated circuits and high-density SRAM. His current work involves the development of the integrated ferroelectric devices. Mr. Uemoto is a member of the Japan Society of Applied Physics.

Masamichi Azuma was born in Chiba, Japan in 1959. He received an M.S. degree in material science from Tsukuba University, Ibaraki, Japan, in 1987. In 1987, he joined Matsushita Electronics Corporation, Osaka, Japan. During 1987-1990 he worked on the CCD imager for HDTV system. Since 1991, he has been a visiting scholar at the University of Colorado at Colorado Springs conducting research in the area of ferroelectric thin films for semiconductor integrated circuits. He is also a visiting researcher at Symetrix Corporation in Colorado Springs. He is the author or co-author of several technical papers in the area of integrated ferroelectrics. He is a co-inventor in many patent disclosures in the area of ferroelectric devices for microwave applications and non-volatile memory applications. Mr. Azuma is a member of the Japan Society of Applied Physics.

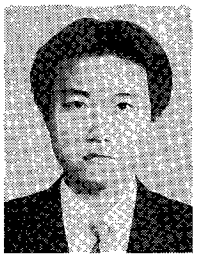


Shinichiro Hayashi was born in Osaka, Japan in 1962. He graduated with a B.S. degree and M.S. in engineering from Kyoto University in Japan. He has been working for Matsushita Electronics Corporation in Osaka, Japan, since 1987. He is a member of the Japan Society of Applied Physics. He is presently a visiting researcher of University of Colorado at Colorado Springs and Symetrix Corporation in Colorado Springs, Colorado, USA. He is the author or co-author of several papers and co-inventor in many patent disclosures in the area of integrated ferroelectric materials, processes, and devices.

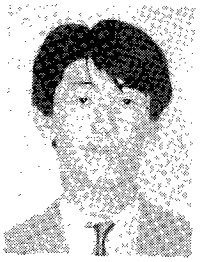
Toru Nasu was born in Kyoto, Japan, on January 9, 1965. He received the B.S. and M.S. degrees in electrical engineering from Osaka Prefecture University in 1988 and 1990, respectively. He joined Matsushita Electronics Corporation in 1990, and is engaged in research on ferroelectric devices.



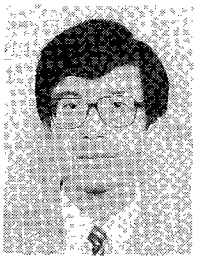
Atsuo Inoue was born in Kyoto on April 30, 1964. He received the B.S. and M.S. degrees in electrical engineering from Kansai University in 1988 and 1990, respectively. He joined Matsushita Electronics Corporation in 1990, and is engaged in research on ferroelectric devices.



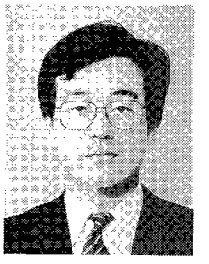
Akihiro Matsuda was born in Nagoya, Japan, on April 16, 1965. He received the B.S. and M.S. degrees in applied physics and physics from Konan University in 1989 and 1991, respectively. He joined Matsushita Electronics Corporation in 1991, and is engaged in research and development of integrated ferroelectric devices. Mr. Matsuda is a member of Japan Society of Applied Physics.



Yoshihisa Nagano was born in Fukuoka, Japan, on August 21, 1966. He received the B.S. and M.S. degrees in electrical engineering from Osaka University in 1989 and 1991, respectively. He joined Matsushita Electronics Corporation in 1991, and is engaged in research and development of integrated ferroelectric devices.

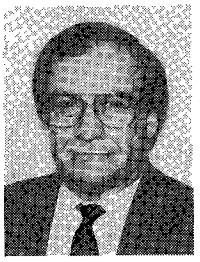


Shin-ichi Katsu was born in Osaka, Japan, on June 11, 1954. He received the B.S. and M.S. degrees in electronics engineering from Osaka University in 1978 and 1980, respectively. He joined Matsushita Electronics Corporation in 1980, where he was engaged in research and development of GaAs IC's and microwave low-noise GaAs FET's. His most recent activities have included development of neural network processors and ferroelectric integrated circuits. He is currently the manager of the Advanced Silicon Device Development Group at the Electronics Research Laboratory of Matsushita Electronics Corporation.

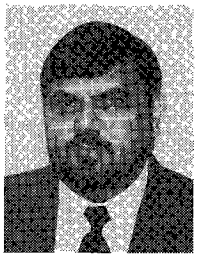


Tatsuo Otsuki was born in Fukui, Japan, on August 17, 1953. He received the M.S. degree in applied physics from the University of Tokyo in 1979. In 1979, he joined the Research and Development Center of Matsushita Electronics Corporation, where he worked on development of dynamic memories. Since 1981, he has been working with Electronics Research Laboratory, Matsushita Electronics Corporation, and has been engaged in development of GaAs high speed devices. He has supervised development activities of CCD image sensors for HDTV camera system. Currently he is a senior engineer of the advanced Si device development group at Electronics Research Laboratory.

Gota Kano received the B.S. degree in 1961 and the Ph.D. degree in 1970, both in electrical engineering from Osaka University, Osaka, Japan. He joined Matsushita Electronics Corporation in 1961, where he has been engaged in the research and the development of semiconductor devices. He was a committee member of International Solid State Circuit Conference, GaAs IC Symposium and is a senior member of IEEE and the Japan Society of Applied Physics. He occasionally gives his lecture at the electrical engineering and the electronics engineering of Osaka University.



Larry D. McMillan was born in Michigan, USA. He received a B.S. in physics and math from Aquinas College in Grand Rapids, Michigan, and a M.S.E.E. degree from Arizona State University. He has nearly thirty years' experience in the microelectronics industry, where he performed duties in engineering, research and eventually senior level management in several companies (Motorola, NCR, Storage Technology, etc.) prior to co-founding Ramtron Corporation and Symetrix Corporation. He holds several patents and is the co-inventor in over 100 disclosures/patent applications in the area of integrated ferroelectrics. He is the author and co-author of over fifty publications in the areas of ferroelectric materials, devices and integration. He is presently president and CEO of Symetrix Corporation in Colorado Springs, Colorado.



Carlos A. Paz de Araujo was born in Natal, Brazil in 1952. He graduated with a B.S.E.E., M.S.E.E, and Ph.D. in 1977, 1979 and 1982 respectively from the University of Notre Dame in Indiana, USA. He is a full professor of Electrical Engineering at the University of Colorado at Colorado Springs. He is also the Director of the Microelectronics Laboratory at the University. He is the author or co-author of over 100 technical papers. He is a co-inventor in over 100 patent disclosures and/or pending applications in the area of Integrated Ferroelectrics. Dr. Araujo is a member of the IEEE, Electrochemical Society, American Ceramic Society, AIP and Materials Research Society.