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Si LSI Process Technology for Integrating Ferroelectric Capacitors

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The fabrication procedure of ferroelectric thin film capacitors onto conventional Si LSIs is investigated. Electrical characteristics of the integrated $Ba_{1-x}Sr_xTiO_3$ (BST) capacitors and the metal-oxide-semiconductor transistors embedded in the Si substrate are examined. Results of these measurements suggest the usefulness of this integration process for the fabrication of ferroelectric thin film devices, which is substantiated by the evaluation of an analog/digital IC with the integrated BST bypass capacitor.

KEYWORDS: ferroelectric, fabrication procedure, metalorganic deposition, $Ba_{1-x}Sr_xTiO_3$, leakage current, time-dependent dielectric breakdown

1. Introduction

Within the last several years, ferroelectric thin films have attracted much attention because of their electronic and electrooptic applications, which has brought about new and significant developments in this field. From the viewpoint of the semiconductor industry, some of the application areas for ferroelectric thin films are of the most recent interest, such as high-density dynamic random-access memories (DRAMs),[1] nonvolatile memories,[2] metal-ferroelectric-semiconductor devices,[3] and LSIs with integrated bypass capacitors.[4] The fabrication procedure of ferroelectric thin film capacitors into conventional Si LSIs, however, is not yet well established, though some laboratories are manufacturing prototype low-density nonvolatile memories.[5]

This paper describes our process technology for integrating ferroelectric thin film capacitors into Si LSIs, which can be applied to various kinds of ferroelectric thin film devices. It should be mentioned that throughout this paper the term "ferroelectric" is used to describe these films even though the hysteresis characteristics provided by spontaneous polarization are not utilized in the devices described later.

2. Integration of Ferroelectric Capacitors on Si LSIs

2.1 *Preparation of ferroelectric thin films*

In this study we chose $Ba_{1-x}Sr_xTiO_3$ (BST) as a high-dielectric material, and the BST thin films were deposited by a spin-on technique called metalorganic deposition (MOD).[1,6] It should be noted here that the capacitor fabrication process below is not affected by the deposition methods of the ferroelectric thin films, such as sputtering,[7] laser ablation,[8] metalorganic chemical vapor deposition (MOCVD),[9] and liquid source CVD.[10] For the preparation of the MOD-derived thin films, a mixture of metal alkoxides corresponding to the required ferroelectric thin films was used in the spin-coating process, followed by the drying and sintering processes.

Figure 1 shows the X-ray diffraction patterns for the BST thin films deposited at different Ba/Sr ratios. These spectra indicate that these films have a polycrystalline phase with no orientation. In comparison with the lattice constant of each BST film, which was calculated from these X-ray peaks, and that of BST ceramics, it is found that the lattice constant of the BST film changes in the same manner as bulk ceramics,[1,6] which suggests crystallographic and electrical similarities between the thin films and bulk ceramics. Since the BST system has the crystal phase transition between tetragonal and cubic at the Sr composition of 0.3,[11] the largest dielectric constant among all of these compositions can be expected at this optimum composition.

2.2 *Fabrication procedure*

A schematic illustration of the fabrication process of the ferroelectric thin film capacitors is shown in Fig. 2. The ferroelectric process layers are formed after the fabrication of the conventional metal-oxide-semiconductor (MOS) transistors onto the Si substrate, where the SiO_2 layer is deposited on the surface.

First, the bottom Pt electrode is vapor-deposited on the substrate. To obtain good adhesion, a Ti layer is formed between the Pt electrode and the substrate.[12] Then, the ferroelectric thin film is deposited on the Pt electrode by the above-mentioned MOD technique.

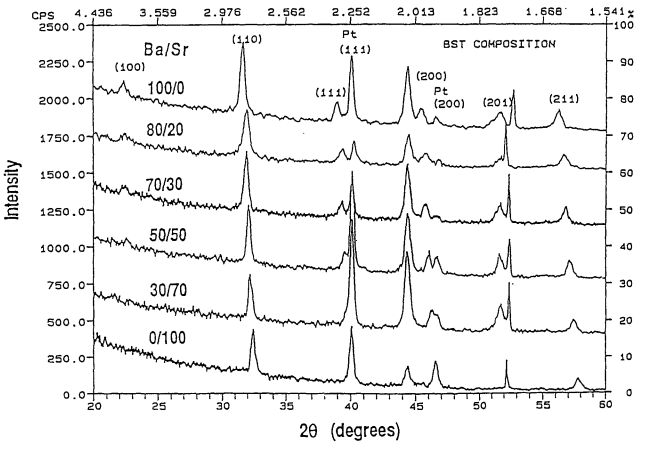


Fig. 1. X-ray diffraction patterns of the $Ba_{1-x}Sr_xTiO_3$ thin films. Sintering temperature: 750°C. Film thickness: 160 nm.

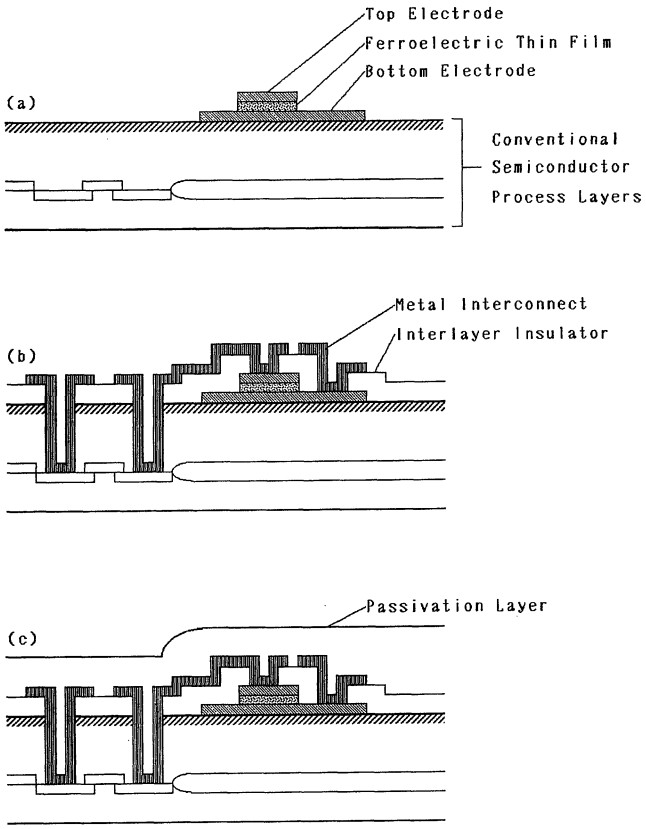


Fig. 2. A schematic illustration of the fabrication process of integrated ferroelectric capacitors.

After that, the top Pt electrode is vapor-deposited on the ferroelectric thin film, and its patterning is carried out with use of the ion milling method or the reactive ion etching (RIE) technique[13] to create the ferroelectric thin film capacitors (Fig. 2(a)).

As an interlayer insulator, a SiO_2 thin film is deposited over the ferroelectric capacitors by CVD. A Ti film is vapor-deposited on the top Pt electrode before the etching of the ferroelectric process layers in order to obtain good adhesion to the CVD-deposited SiO_2 layer.

The subsequent fabrication process, which consists of the metallization process for the interconnection (Fig. 2(b)) and the passivation process followed by the formation of bonding pads (Fig. 2(c)), is equivalent to the standard Si LSI process. It should be noted that in the metallization process a barrier layer is required between Al and Pt because Pt tends to react with Al to form Al_2Pt, whose growth sometimes causes the metallization degradation. Currently we employ TiW as a barrier metal. As a passivation layer, Si_3N_4 is deposited by plasma CVD at present.

Figure 3 shows the scanning electron micrograph of the integrated $Ba_{0.7}Sr_{0.3}TiO_3$ (BST(70/30)) thin film capacitor. For the patterning of this BST capacitor, the RIE technique was utilized.

2.3 *Characteristics of integrated ferroelectric capacitor*

For electrical characterization of the integrated ferroelectric thin film capacitors, BST(70/30) capacitors

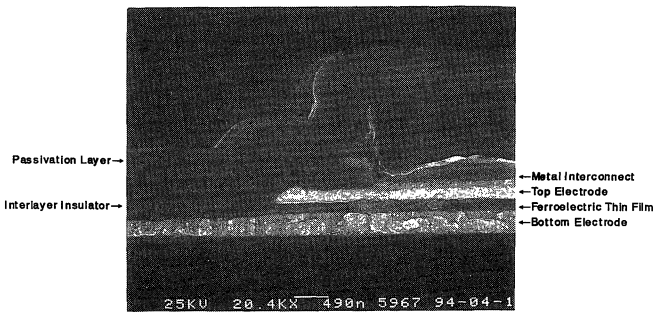


Fig. 3. Scanning electron micrograph of the integrated $Ba_{0.7}Sr_{0.3}TiO_3$ capacitor. Due to the limit of sensitivity of our instrument, the boundary between the interlayer insulator (SiO_2) and the passivation layer (Si_3N_4) is not clear.

were formed onto the Si substrate where MOS transistors had already been fabricated, using the above-mentioned procedure. Figure 4 shows the leakage current characteristics of the integrated MOD-deposited 180 nm BST(70/30) capacitor measured at room temperature. The leakage current density was around 1.2×10^{-7} A/cm^2 at 1 V. This suggests that the integrated BST capacitor is applicable to highly integrated memories such as 256M DRAM. Its time-dependent dielectric breakdown (TDDB) characteristic is shown in Fig. 5, which was taken at 125 °C. From the extrapolation of the experimental results in the same manner as the case of SiO_2, the lifetime to breakdown of the cell capacitor is concluded to be over 10 years even under a stress voltage of 5 V. These results indicate the suitability of the integrated BST capacitors for electrical use, which is also supported by the results of the measurements of other electrical properties of the integrated BST capacitors.

Electrical characteristics of the embedded MOS transistors were also examined, which reveal that these transistors are not damaged by this integration process. This indicates the compatibility of this process with conventional semiconductor processes.

3. Application to Integrated Bypass Capacitor

To demonstrate the validity of the integrated ferroelectric thin film capacitors, we have experimentally fabricated an analog/digital Si IC which integrates about 3800 transistors, and the BST(70/30) capacitor which functions as a bypass capacitor. By building the bypass capacitor which must have a large capacitance (on the order of hundreds pF) in a chip, the supply voltage is effectively stabilized and the electronic noise is reduced.[14] Reduction of external pins and external bypass capacitors and decrease of the package size are also expected.

The capacitance of this integrated BST capacitor was 1400 pF. The analog/digital Si IC with a conventional 40 pF SiO_2 bypass capacitor instead of the BST bypass capacitor was also fabricated as a reference. Comparing the waveforms of the supply voltages shown in Figs. 6(a) and 6(b), fluctuation of the supply voltage is seen to be effectively suppressed with use of the integrated BST bypass capacitor. According to the frequency analysis, integrating the BST(70/30) bypass

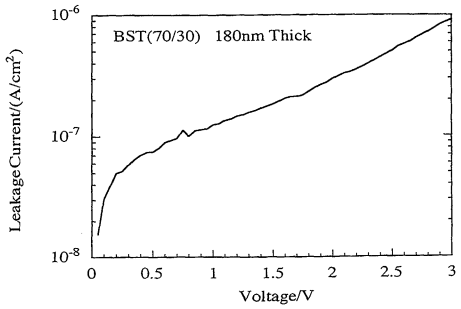


Fig. 4. The leakage current characteristics of the integrated $Ba_{0.7}Sr_{0.3}TiO_3$ capacitor measured at room temperature. Film thickness: 180 nm.

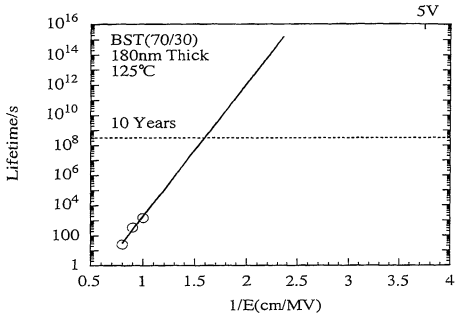
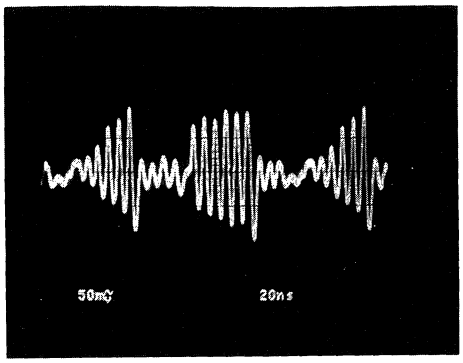
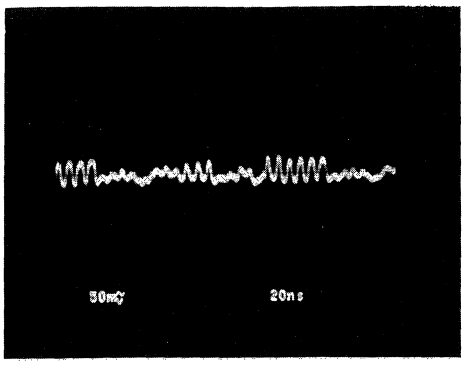


Fig. 5. TDDB characteristics of the integrated $Ba_{0.7}Sr_{0.3}TiO_3$ capacitor measured at 125 °C. Film thickness: 180 nm.



(a)



(b)

Fig. 6. (a) The waveform of the supply voltage of the Si IC with the 40 pF SiO_2 bypass capacitor. (b) The waveform of the supply voltage of the Si IC with the 1400 pF integrated $Ba_{0.7}Sr_{0.3}TiO_3$ capacitor.

capacitor leads to a 70% decrease in the amplitude of electronic noise, in comparison with the conventional IC with the SiO_2 bypass capacitor. This indicates that the BST bypass capacitor effectively reduces the electronic noise from signal processors, which is now a serious concern for digital equipment.

4. Conclusions

The fabrication procedure of ferroelectric thin film capacitors onto conventional Si LSIs has been presented. Through device characterization of the integrated ferroelectric capacitors themselves and the Si LSIs with the integrated ferroelectric bypass capacitors, the validity of integrating ferroelectric thin film capacitors on Si devices has been clarified.

The use of ferroelectric thin films, which can be realized by this fabrication process, will be a promising method of producing various new kinds of semiconductor devices.

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