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Ferroelectric Nonvolatile Memory Technology and Its Applications

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Nonvolatile memory utilizing ferroelectric material is expected to be the ultimate memory due to its theoretical low power operation and fast access. We integrated a ferroelectric thin film using a standard complementary metal-oxide-semiconductor (CMOS) process and evaluated its basic characteristics and reliability including endurance and imprint effect. The film was prepared using a spin-on sol-gel method. A ferroelectric thin film formed using liquid source misted chemical deposition (LSMCD) was found to have almost the same characteristics as those of the film formed by the sol-gel method. No effects of the ferroelectric process on the CMOS transistors were observed. Design of ferroelectric memory cells and applications of the ferroelectric nonvolatile memory have been reviewed.

KEYWORDS: ferroelectric, integrated ferroelectronics, $SrBi_2Ta_2O_9$, endurance, imprint, nonvolatile memory, RFID tag, embedded microcontroller

1. Introduction

Ferroelectric material for nonvolatile memory has been researched and developed since the middle of the 1980s mainly in the U.S.A.[1] It is known that the material has a perovskite crystal structure with bistable states, each of which corresponds to logic state "1" or "0". One of the best known perovskite materials is lead titanate-zirconium (PZT). However, it is known to suffer from fatigue[2] defined as a decrease in polarization after repeated switchings. Many studies have been carried out on fatigue and recently its cause has become clearer.[3–5] Meanwhile conductive oxides such as IrO or RuO have been proposed as electrodes for ferroelectric thin films to compensate for this disadvantage of PZT.[6–8] In the 1990s a new ferroelectric material, Bi based layered perovskite oxide, $SrBi_2Ta_2O_9$, known as "Y1",[9] which has a different microstructure and improved fatigue properties was invented. Here we describe the integration of ferroelectric material to a standard complementary metal-oxide-semiconductor (CMOS) process, its characteristics including reliability, cell design for a ferroelectric nonvolatile memory and its applications.

2. Integration of Ferroelectric and CMOS

A ferroelectric process for ferroelectric capacitor formation is carried out on a standard CMOS underlayer consisting of transistors and inter-layer dielectric, and then followed by interconnection and passivation. The maximum temperature during the ferroelectric process is 800°C. A cross-secti onal view is shown in Fig. 1. Figure 2 shows the n-channel and p-channel threshold voltages with and without the ferroelectric process. Their deviations are within the range expected due to process variations so it can be concluded that the ferroelectric process does not influence the CMOS transistor characteristics. Therefore, the standard CMOS process can be used for the integrated ferroelectric. This is the great advantage of the ferroelectric memory compared with the electrically erasable and programmable read only memory (EEPROM) or the dynamic random access memory (DRAM) that require dedicated CMOS process steps, because the ferroelectric process can be treated as an optional step in a standard CMOS process and a ferroelectric nonvolatile memory can be prepared as a standard cell.

There are various techniques for ferroelectric thin film deposition, such as the spin-on sol-gel method, LSMCD, sputter deposition and metalorganic chemical deposition. We chose the spin-on sol-gel method shown in Fig. 3. We believe it is the closest technique to production use because the spin-on method is commonly used in semiconductor factories. The source material, which is a solution in the spin-on method, can be adjusted so that it has an arbitrary composition of metalorganic components in a ferroelectric material. The source material is coated on the electrode, dried to evaporate solvents and then crystallized in oxygen. This method gives poor step coverage but allows the stoichiometry to be controlled and has a short turn-around time. It is suitable for low-to middle-density devices.

Figures 4 and 5 show the remnant polarization and

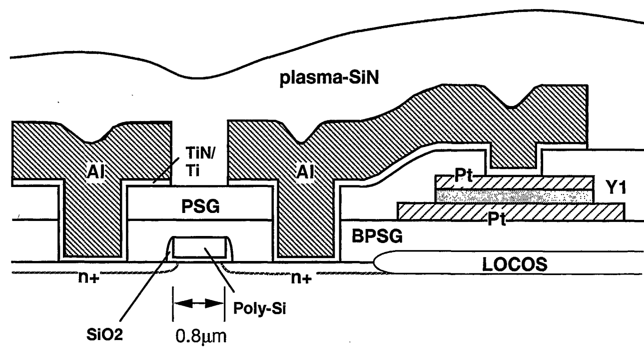

Fig. 1. Cross-sectional view of integrated ferroelectronics with 0.8 μm design rule.

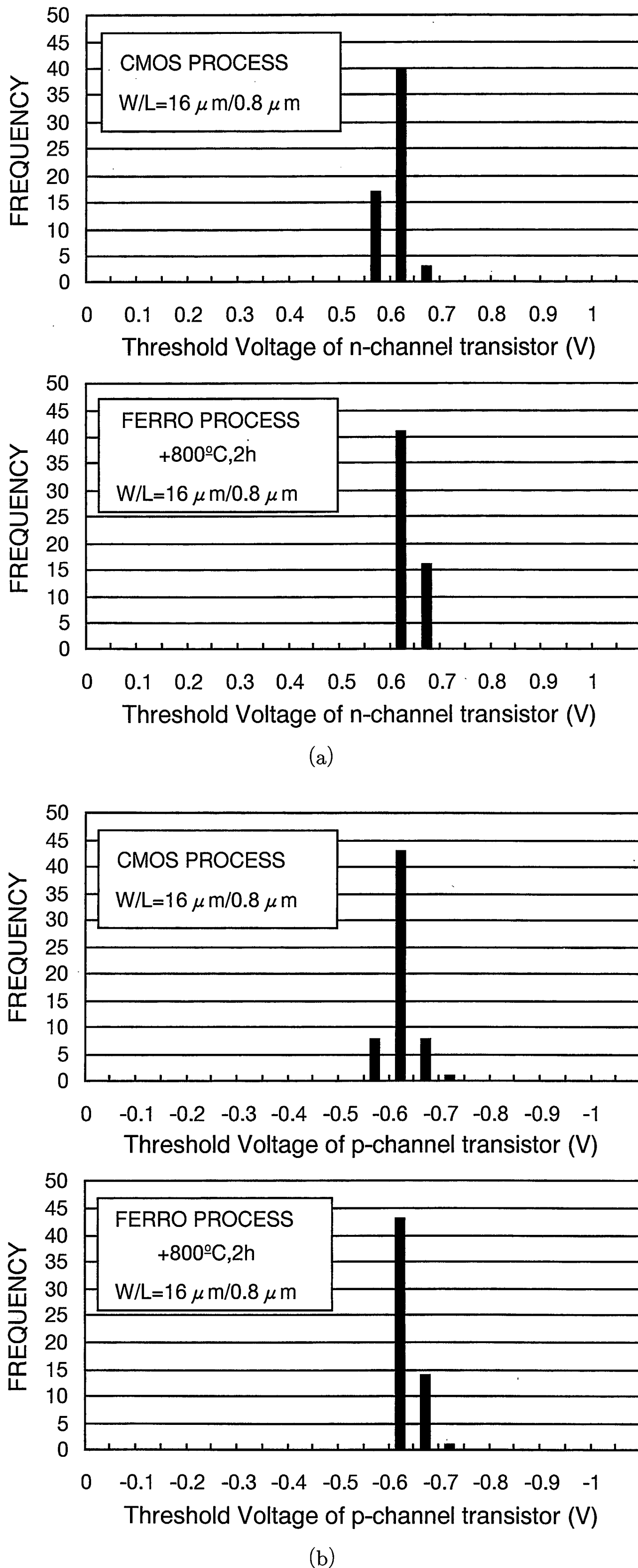

Fig. 2. Influence of ferroelectric process on CMOS transistors in terms of n-channel and p-channel threshold voltages.

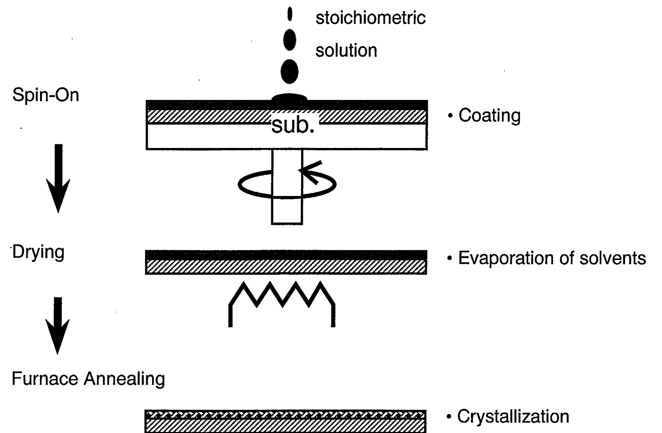

Fig. 3. Sol-gel spin-on process flow for ferroelectric thin-film deposition.

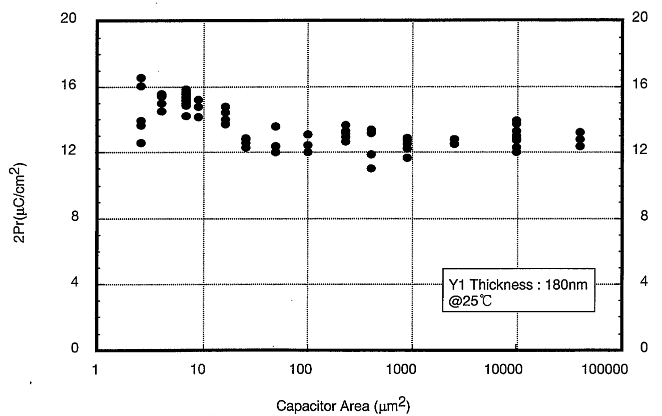

Fig. 4. Remnant polarization characteristics of ferroelectric capacitors as a function of capacitor area.

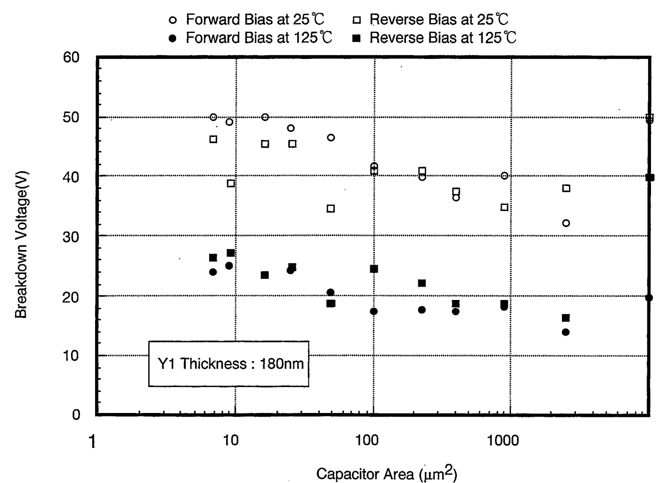

Fig. 5. Breakdown voltage characteristics of ferroelectric capacitors as a function of capacitor area.

breakdown characteristics of ferroelectric capacitors that have undergone all processes. According to the data, the characteristics are almost independent of capacitor area and sufficient charge can be obtained for a memory cell as large as 4 Mbit. Also the bias direction is independent of breakdown voltage. Fig. 6 shows current-voltage characteristics of the capacitors. Identical curves were obtained for capacitors with different areas.

Ferroelectric thin film is easily degraded by hydrogen generated during the fabrication process and so recovery annealing in oxygen is important and a low-hydrogen-concentration process is required.

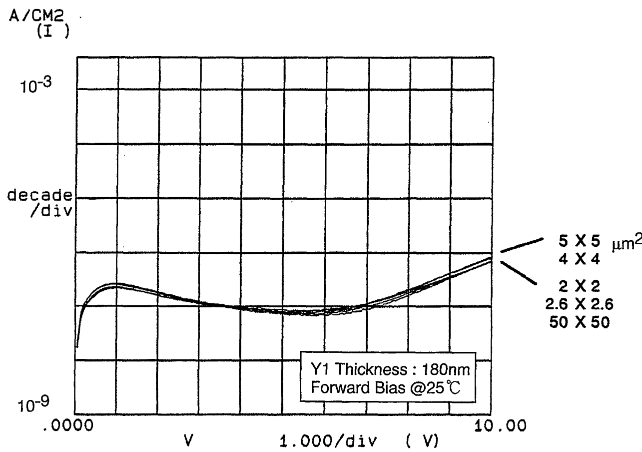

Fig. 6. *I-V* characteristics of ferroelectric capacitors.

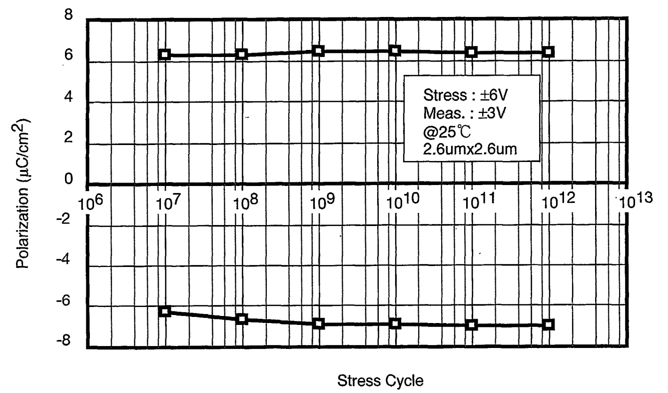

Fig. 7. Endurance characteristics of a ferroelectric capacitor.

3. Reliability of Ferroelectric Capacitor

One of the reliability concerns for ferroelectric capacitors is fatigue. The fatigue-free number of write cycles of a ferroelectric capacitor is much greater than that of an EEPROM, which is typically between 10^4 and 10^6. However, in a ferroelectric memory the capacitor is switched not only by a write operation but also by a read operation, the so-called destructive read. Fatigue is a great problem in PZT-based ferroelectric nonvolatile memories. On the other hand, Bi based layered perovskite oxide, $SrBi_2Ta_2O_9$, is not affected by oxygen vacancies which are considered to be one of the causes of fatigue, due to its layered perovskite oxide structure and it shows good fatigue-free characteristics as shown in Fig. 7.

Ferroelectric material is known to have "imprint" characteristics.[10] Imprint describes the phenomena in which after repeated application of unipolar pulses or DC voltage or after high-temperature storage, the hysteresis curve shifts with the electric field axis, as shown in Fig. 8. If an offset bias is applied to a capacitor with imprint and the hysteresis curve is measured, the curve agrees well with the initial curve as shown in Fig. 9. This implies that imprint is a results of the fixed polarization and its internal field which remains even at zero external voltage. This characteristic should be taken into account when designing memory cell circuits.

4. Memory Cell Design

Ferroelectric nonvolatile memories to date have mainly used a 2T2C cell configuration consisting of two transistors and two capacitors per bit. The cell operation is stable because of the complementary operation of a pair consisting of 1 transistor and 1 capacitor.

However, a cell consisting of 1 transistor and 1 capacitor (1T1C) per bit is required for high-density memory. The 1T1C cell requires a reference cell that generates a reference voltage for which amplifies small signals. We propose a preset reference cell which guarantees a zero voltage condition on the reference cell regardless of the bias conditions.[11] Considering the necessity of coincidence between the characteristics of the reference cell and the memory cell in terms of temperature dependence and cell area deviation, it is desirable to use a ferroelectric

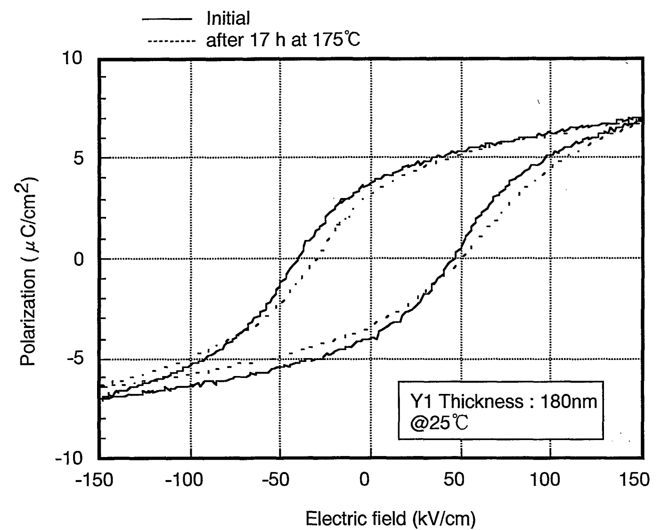

Fig. 8. Hysteresis curve with imprint characteristics after high-temperature storage.

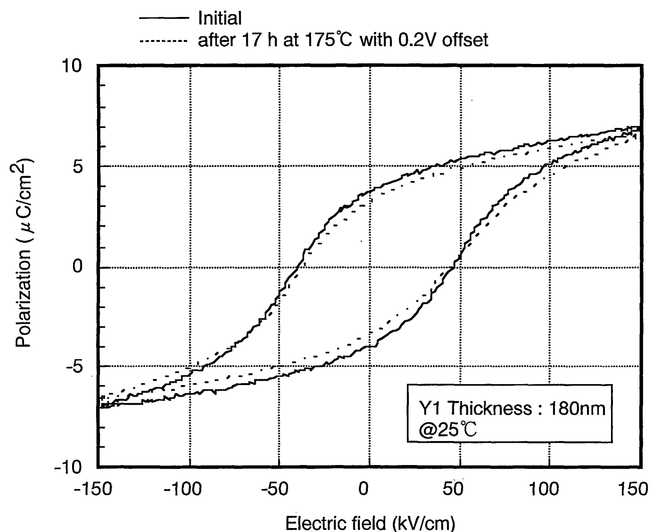

Fig. 9. Imprinted hysteresis curve with offset bias.

capacitor as the reference cell. Ferroelectric thin films exhibit the "relaxation" effect, that is, degradation of polarization after applied voltage becomes zero, as shown

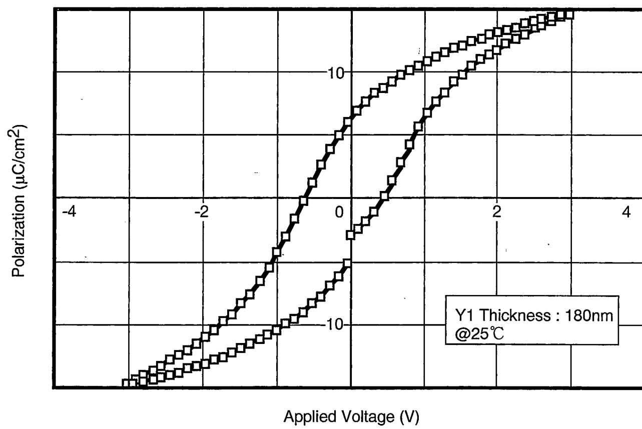

Fig. 10. Remnant polarization relaxation characteristics of a ferroelectric capacitor.

in Fig. 10. According to our study the time constant of the relaxation is in the order of one millisecond. It is necessary to consider this relaxation when designing the memory and reference cells as well as their dependence on applied voltage and temperature. The ratio of bitline parasitic capacitance to equivalent cell capacitance determines the sensing voltage on a bitline. We have to consider this ratio, especially in the case of a low-density memory in which the bitline capacitance is relatively small resulting in a small sensing voltage. In these areas research on an accurate circuit model for a ferroelectric capacitor is very important.

5. Advanced Technology for High-Density Memory

One possible ferroelectric thin-film deposition method for high-density devices is LSMCD.[12] In Fig. 11 a single solution is misted, carried to a chamber by Ar carrier gas and deposited on a substrate. The drying and crystallization processes conform to those of the spin-on method. LSMCD has better step coverage than the spin-on method, which is essential for higher integration. The two methods allow the same controllability of stoichiometry because of the single liquid source. Figures 12 and 13 show the remnant polarization and I-V characteristics of ferroelectric capacitors fabricated by LSMCD. Almost the same properties as those of the capacitor fabricated by the sol-gel method have been obtained.

6. Applications of Ferroelectric Memory

Ferroelectric nonvolatile memory is suitable not only for stand-alone memories but also for embedded memories because of its low power requirement, fast access time and potentially low cost. A radio frequency identification (RF-ID) tag IC is one of the possible applications. The IC generates DC voltage by rectifying the carrier electromagnetic field and accesses on-chip ferroelectric nonvolatile memory to read and write using the DC power. The communication range is determined by the power consumption of the IC. The range is greater for a ferroelectric-memory-based RF-ID tag than for a tag with EEPROM since the former consumes less power and operates at a lower supply voltage in weak electromagnetic fields (Fig. 14).

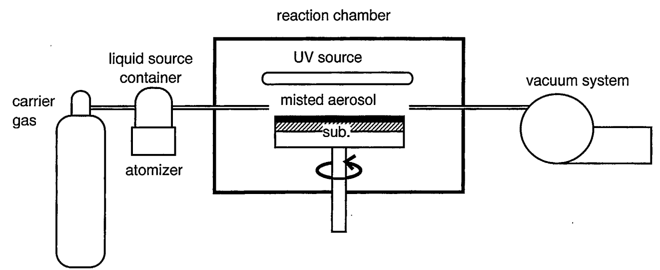

Fig. 11. Liquid source misted chemical deposition method (LSMCD).

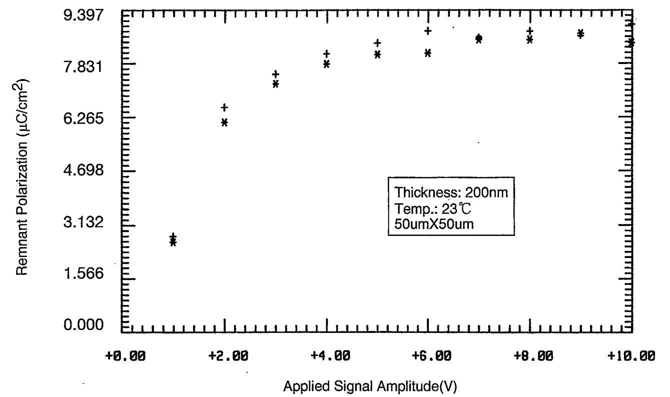

Fig. 12. Remnant polarization characteristics of a ferroelectric capacitor prepared by LSMCD.

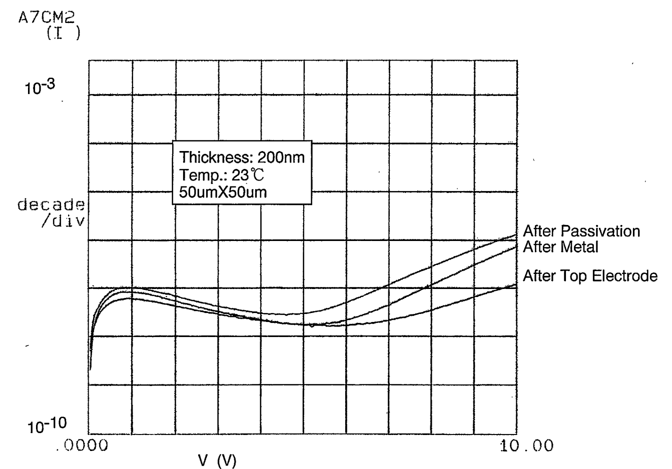

Fig. 13. I-V characteristics of a ferroelectric capacitor prepared by LSCMD.

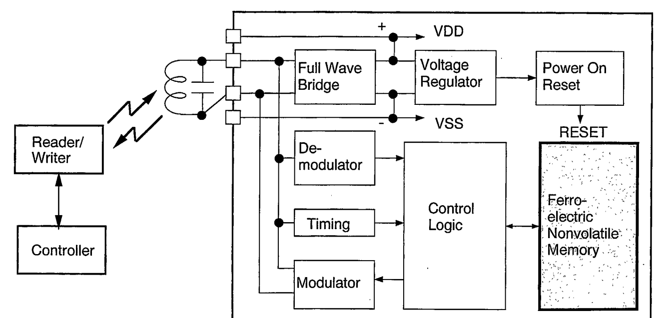

Fig. 14. RF-ID IC application of a ferroelectric nonvolatile memory.

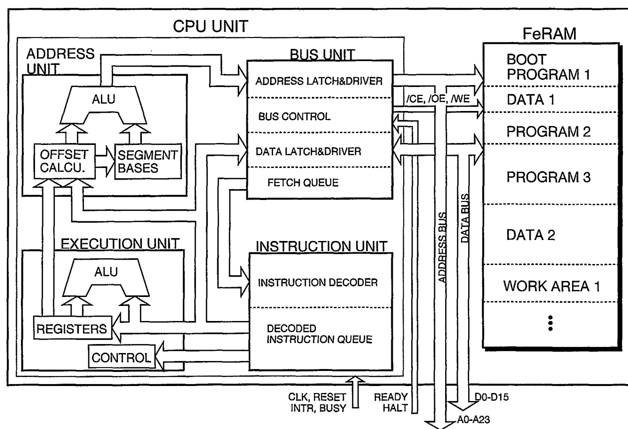

Fig. 15. A ferroelectric nonvolatile memory embedded microcontroller.

Another application is the ferroelectric memory embedded microcontroller.[13] The microcontrollers constructed to date have an EEPROM as a reprogramable memory and a full CMOS static random access memory (SRAM) for data processing on the chip. SRAM has a large cell area and EEPROM cannot be used as a data memory due to its slow write speed. To obtain a chip with different SRAM to EEPROM memory capacity ratio, it must be redesigned. A ferroelectric-memory-embedded microcontroller (mcu) as shown in Fig. 15 has good flexibility because it uses the ferroelectric memory as the main memory. The memory area is used for the boost program, as a data area and as a work area, but there is no physical division between these areas. It is not necessary to design a great variety of microcontroller chips. Furthermore it is possible for the microcontroller to have an evolving program by implanting a nesting function inside the program itself which generates new program data.

7. Summary

We described ferroelectric thin-film deposition technology, its characteristics, ferroelectric memory cell design and the applications of ferroelectric memory. Compared with semiconductor technology, ferroelectric technology requires further research and development, but we believe that it will have a very important role in the field of semiconductor devices due to its superior characteristics.

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