Integrated Ferroelectrics, 1997, Vol. 17, pp. 21-30
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Printed in India

NON-VOLATILE MEMORIES USING $SrBi_2Ta_2O_9$ FERROELECTRICS

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Ferroelectric non-volatile memories (FENVM) are fabricated using spin-coat and fire deposition of the $SrBi_2Ta_2O_9$ layered perovskite ferroelectric. Test memories using a 2 transistor-2 capacitor bit cell, top contacts to capacitors and single level metal were fabricated. We report here on the integration and electrical characteristics of fully functional 1 Kbit test memories.

Keywords: ferroelectric; non-volatile memory; process integration

INTRODUCTION

In comparison with conventional floating gate non-volatile memories (EEPROM and Flash EEPROM), ferroelectric non-volatile memories

(FENVM) offer much higher speed write and substantially lower write voltages. These attributes make FENVMs especially attractive for low-power applications and applications with non-volatile write speed is critical, especially portable devices such as pagers, smartcards, and cellular phones.

We report here on the process integration and electrical performance of 1 Bit test memories. As shown in Fig. 1, a 2 transistor-2 capacitor bit cell is used to provide complementary data storage and easier data sensing. The drive lines run parallel to the word lines which avoids the disturb that occurs in circuits with the drive lines parallel to the bit lines.

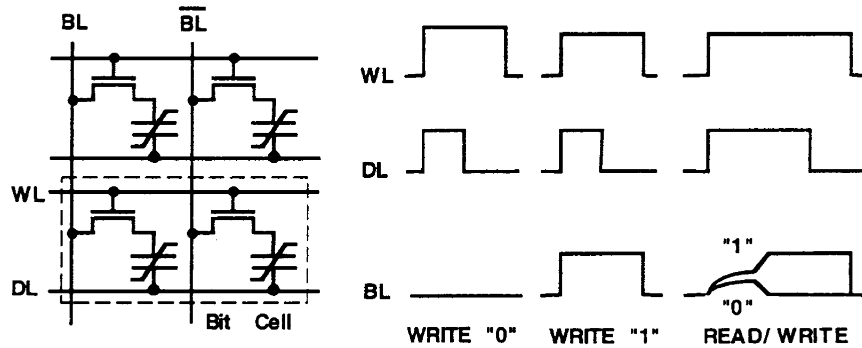

FIGURE 1. Schematic of 2T-2C bit cell array and sensing.

PROCESS INTEGRATION

The process sequence for the test memory fabricates the ferroelectric capacitor module following the formation of the CMOS transistors and prior to the formation of the metal interconnection. $SrBi_2Ta_2O_9$ (SBT) is used as the ferroelectric material because of its demonstrated high reliability[1-4]. The ferroelectric films were deposited with a spin-on technique[5,6] using SBT solutions with 10% excess Bi prepared from 2-ethylhexanoate precursors. Although most of the organics decompose below below 300 °C, firing above 500 °C is required to remove carbonaceous residues. Following spin-coat, the films were

first heated at 200-400 °C on a hot plate and then further densified at 650 - 800 °C. Multiple coat-fire processes are used to achieve the desired 200 nm film thickness for the intended 3 V operation. The film roughness is a function of the annealing temperature. RMS film roughness vs temperature as determined by AFM is shown in Fig. 2 along with an SEM of a well crystallized film. XRD studies show that temperatures of 750 °C or above are required to achieve full crystallization. During the crystallization process the SBT grains tend toward a spherical shape which results in a relatively rough film surface. Sputtered Pt electrodes were used and the bottom electrode used a TiO_2 adhesion layer to the underlying interlevel dielectric. XRD shows the Pt bottom electrode to have a (111) orientation but no preferred orientation is observed in the SBT film. The capacitors were patterned using ion milling. The incident ion beam angle and other process parameters must be optimized to avoid problems with redeposition of the etched materials on the sidewalls of the photoresist and the capacitor dielectric[7]. An oxygen anneal is used following the capacitor patterning to recover degradation of the ferroelectric properties. Following formation of the capacitors, they are covered with a capacitor level dielectric (CLD). Contact openings to the capacitors and the other circuit elements are photolithographically defined and etched. We have previously reported[8] that process damage is observed following plasma enhanced CVD of the CLD and RIE patterning of the contact openings. Under appropriate conditions a subsequent oxygen anneal can result in nearly complete recovery of ferroelectric properties. A conventional Al/TiN/Ti metallization stack is then deposited and etched to form the interconnection. In the integration architecture used here, metal interconnect contacts are made to both bottom and top electrodes. The TiN acts a diffusion barrier as a diffusion barrier between the aluminum metallization and the Pt electrodes as well as serving its standard function of a diffusion barrier between aluminum and silicon. During the plasma etching to pattern the interconnect, damage to the capacitors can occur due the antenna effect of the metal patterns.[9] The degree of damage to capacitors is dependent on the circuit layout. An example of dependence of the damage on the ratio of the metal area to capacitor area is shown in Fig. 3. Both the large and small capacitors are connected to the same size

of probe pad (approximately 100 μm x 100 μm). A combination of appropriate circuit design and careful control of etch processes including over-etch can be used to control such charge damage. With properly optimized process integration, any degradation of ferroelectric properties can be controlled as illustrated in Fig. 4.

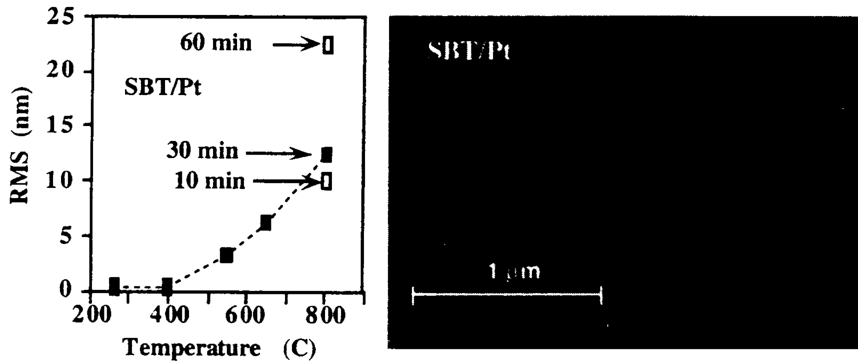

FIGURE 2. (a) Film roughness as a function of anneal temperature and time, and (b) SEM of well crystallized SBT showing the spherical nature of the grains.

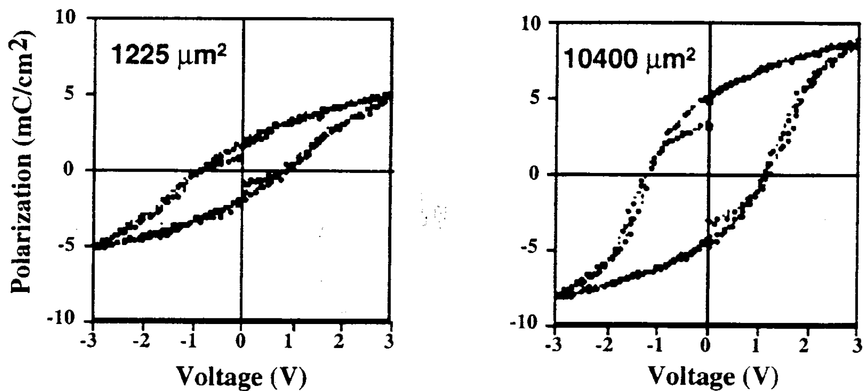

FIGURE 3. Charging etch process damage to (a) a 1225 μm^2 capacitor and (b) a 10400 μm^2 capacitor.

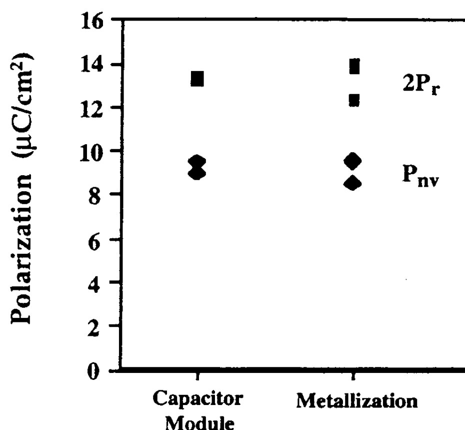

FIGURE 4. Ferroelectric properties following capacitor formation and metallization processes showing limited process damage.

RESULTS

A photomicrograph of a completed 1 Kbit test FENVM is shown in Fig. 5. The memory array is seen in the center of the chip photo. The array efficiency will increase when higher density memories are designed for product applications. Figure 6 shows SEMs of a top view of a completed memory bit cell and a focused ion beam (FIB) prepared cross section thorough a bit cell capacitor and metal strap connection to a transistor source/drain.

The fully integrated FENVM wafers show some modest shifts in transistor properties of parametric test structures compared to those of control wafer processed without the ferroelectric capacitor module. On the FENVM wafers the short n-channel transistors (0.8 to 1.2 μm gates) show a 70 mV increase in Vt while the p-channel transistors only show a shift of 20 mV toward less negative values. Equal area arrays of different sized individual capacitors shows an edge or size effect (Fig. 7). This effect does not seriously affect the relatively large

bit cell capacitors used in this test memory, but the edge or size effect must be resolved for development of high density memories.

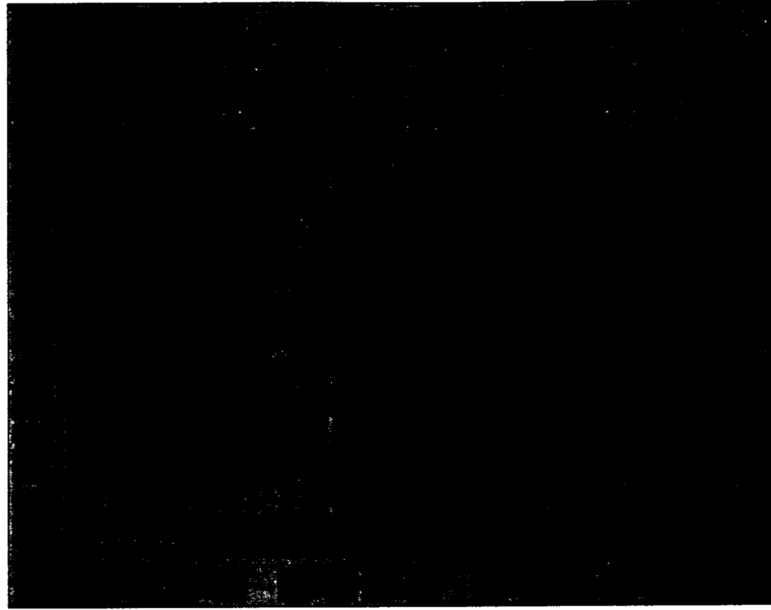

FIGURE 5. Micrograph of 1 Kbit FENVM test chip.

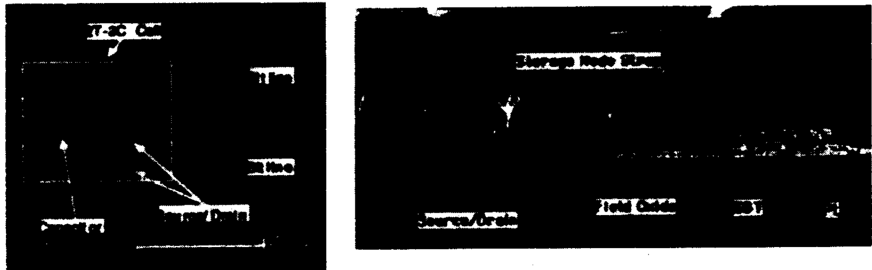

FIGURE 6. (a) SEM top view with 2T-2C bit cell outline, and (b) SEM cross-section of bit cell. The bit cell capacitors in the 2T - 2C bit cell each have an area of 17.5 μm^2, and the area of the bit cell is 181 μm^2.

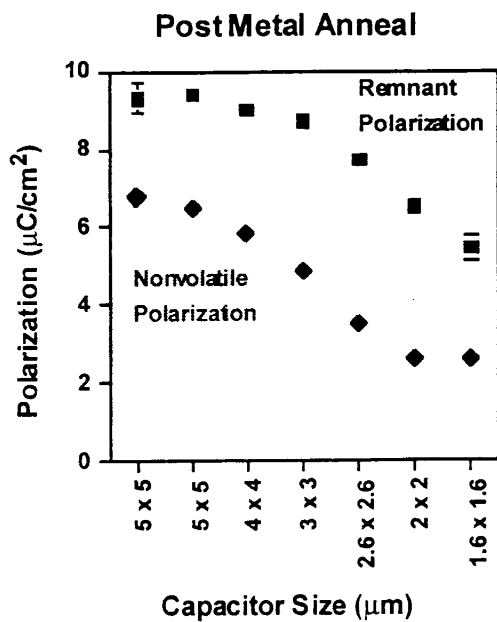

FIGURE 7. Polarization as a function of capacitor size.

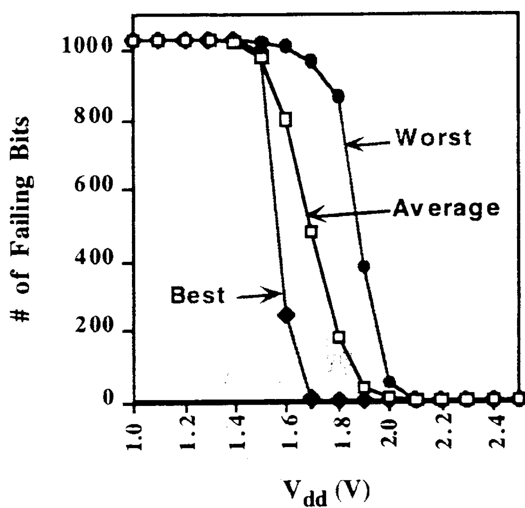

FIGURE 8. Yield fall out as a function of voltage.

Fully functional 1 Kbit memories were obtained. The circuit shows exceptionally good performance at low voltage. The circuit was designed to operate at 3 V and no internal charge pumping is employed. There is no use of a word line boost. The memories are quite robust to voltages even lower than the design voltage. Fully functional memories were observed to about two volts operation as illustrated in Fig. 8.

Reliability is an important factor for a non-volatile memory. We have explored the acceleration of fatigue in SBT capacitors using both voltage[6] and temperature[7] acceleration. For 3 V bipolar signals, no fatigue is observed to 10^{12} cycles for temperature up to and including 125 °C, however, at 175 °C the onset of fatigue is observed at about 10^{10} cycles. High voltages can also accelerate fatigue. Figure 9 shows that even under 6 V operation, 200 nm thick SBT capacitors do not show any fatigue at room temperature to 10^{11} cycles. Under 8 V stressing, the onset of fatigue is observed at about 10^{9} cycles.

Data retention following a write is an important reliability factor for non-volatile memories. Retention test on the 1 Kbit test memories following a 2000 hr retention test showed some memories with on bits failing for retention. However, other memories did show loss of retention on a small number of bits. Additional effort is required to understand and improve the retention.

DISCUSSION

There are selected market opportunities for relatively low-density FENVMs based on their low power and fast write speeds. However, higher-density memories at 1 Mbit and beyond will open much larger markets to FENVMs. To achieve competitive bit cell sizes with flash EEPROM memories, FENVMs need to use a process integration architecture where the capacitor is stacked over a contact to a source/drain of the bit cell access transistor. This requires the development of appropriate electrode/barrier/contact plug materials technologies that can withstand the high-temperature oxygen processing of ferroelectric dielectrics. Additionally the array architecture needs to employ a 1T-1C bit cell. The area or edge effects

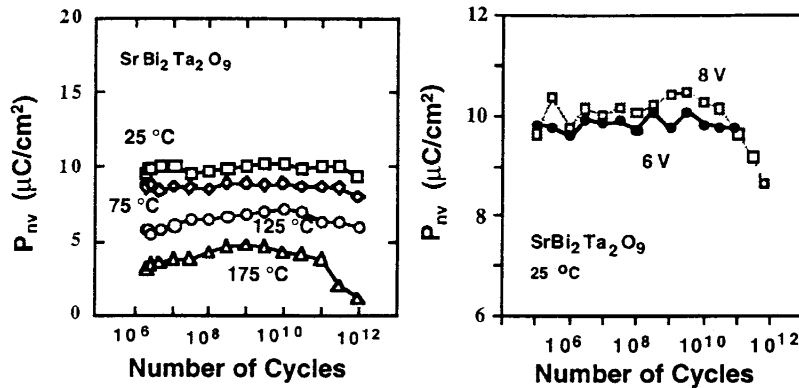

FIGURE 9. Accelerated fatigue test results.

in ferroelectric capacitors must be reduced to allow the bit cell capacitors to shrink as design rules become smaller. Reliability enhancement also is needed for FENVMs to compete against a wide selection of non-volatile memory applications where 10 year retention time is the standard. Eventually, with continued circuit shrinking, planar ferroelectric capacitors will not provide enough signal for robust sensing and 3-dimensional capacitors will be required. Such 3-dimensional capacitors are already being investigated for BST DRAM applications[10]. Another area that requires enhancement is ferroelectric circuit simulator models[11,12] that can account for the relaxation as well as the non-linear, hysteretic behavior observed in ferroelectric capacitors. This will require better physical models of the relaxation effects in ferroelectric capacitors.

Acknowledgements

The authors would like to thank Mike Kottke, Rich Gregory and Tom Lii for their technical contributions to this work. We also gratefully acknowledge the technical assistance of Darrell Roan, David Gentile, Linda Massirer, Matthew Smith, and William Dennig.

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