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Ferroelectric Memory Circuit Technology and the Application to Contactless IC Card

Koji ASARI†a), Hiroshige HIRANO††, *Members*, Toshiyuki HONDA††, Tatsumi SUMI†, Masato TAKEO††, Nobuyuki MORIWAKI††, George NAKANE†, Tetsuji NAKAKUMA††, Shigeo CHAYA††, Toshio MUKUNOKI†††, Yuji JUDAI††, *Nonmembers*, Masamichi AZUMA†, *Member*, Yasuhiro SHIMADA†, *and* Tatsuo OTSUKI†, *Nonmembers*

SUMMARY Ferroelectric non-volatile memory (FeRAM) has been inspiring interests since bismuth layer perovskite material family was found to provide "Fatigue Free" endurance, superior retention and imprint characteristics. In this paper, we will provide new circuits technology for FeRAM developed to implement high speed operation, low voltage operation and low power consumption. Performance of LSI embedded with FeRAM for contactless IC card is also provided to demonstrate the feasibility of the circuit technology.

key words: *FeRAM, high speed, low voltage, low power consumption, non-volatile, contactless IC card*

1. Introduction

Ferroelectric non-volatile memory (FeRAM) have excellent characteristics in terms of low power consumption and high speed write which have not been achieved with conventional non-volatile memory technology such as EEPROM. Table 1 shows a comparison between FeRAM and other type of memories. It is noted that FeRAM has the capabilities of high operation speed in the range of DRAM and the small cell size which is almost the same as DRAM if the same process rule is applied to the design. Furthermore, the endurance cycle of FeRAM is counted up to 10^{13} cycles and is expected to reach 10^{15} cycles in the future. As for the cell size, FLASH EEPROM gives the smallest cell for 1T memory cell (1 transistor per bit) structure. However, an FeRAM with 1T memory cell structure is demonstrated recently by using ferroelectric material on the gate oxide of pass transistor [1]. This indicates that FeRAM has a feasibility of mass storage memory as well as non-volatile RAM. In other words, FeRAM is expected to open a new era of semiconductor memory.

The above features of FeRAM are derived from utilizing unique characteristics of ferroelectric material. Perovskite crystal structure in Fig. 1 is the simplest crystal structure which exhibits ferroelectricity. The spontaneous polarization of ferroelectric materials is caused by a displacement of the cation, A and B against the anion, oxygen in this case. As the direction of the polarization is altered by applied electric field, FeRAM using ferroelectric memory cell capacitor can write logic state of "1" and "0" by changing the direction of applied voltage. The electric field required for the displacement is usually around 100 kV/cm which is equivalent to only 2 V with a film thickness of 100 nm, and the polarization reversal, writing of FeRAM, is easily performed within 100 ns. This physical mechanism is the origin of the superior features of FeRAM. On the other hand, EEPROM writes logic states by changing threshold voltage of memory cell MOS transistor. An electron injection into the floating gate of the MOS transistor through very thin silicon dioxide gate film is needed to shift the threshold voltage. This requires high voltage (12 V) and long

Table 1 The comparison FeRAMs with other memories.

	FeRAM	FLASH	SRAM	DRAM
Write Voltage(V)	3V	12V	3V	3V
Write Cycle(s)	100n	10 μ	10n	60n
Endurance	$>10^{13}$	10^{6}	no limit	no limit
Cell size	1	0.8	4	1

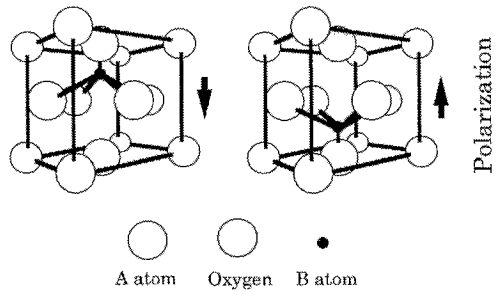

Fig. 1 Perovskite structure.

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† The authors are with Electronics Research Laboratory, Matsushita Electronics Corporation, Takatsuki-shi, 569-1193 Japan.
†† The authors are with ULSI Process Technology Development Center, Matsushita Electronics Corporation, Kyoto-shi, 601-8413 Japan.
††† The author is with Corporate Semiconductor Development Division, Matsushita Electric Industrial CO., LTD, Osaka-shi, 570-8501 Japan.
a) E-mail: asari@erl.mec.mei.co.jp

write cycle time ($>10\ \mu s$).

Even with the substantial advantages of FeRAM over the conventional EEPROM, a successful commercialization of FeRAM relies upon further development of circuit design and device architecture. This paper discusses the circuit technology that is devised for FeRAM to achieve the above purpose. Performance of an FeRAM embedded LSI for contactless IC card developed by incorporating our design scheme is also given to demonstrate the feasibility of FeRAM based device.

2. FeRAM Circuit Operation

The operation of conventional circuit is described below. There are two types of memory cell, one is 2T/2C type (2 transistors and 2 capacitors) and the other is 1T/1C type (1 transistor and 1 capacitor).

The 2T/2C type memory cell and a read scheme of FeRAM with 2T/2C cell are shown in Fig.2 and Fig. 3. When the word line (WL) and the CP of the selected cell are driven to H (V_{cc} voltage) during a read operation, electric charge of a cell comes out to bit lines (BL and /BL). The difference in voltage between BL and /BL is amplified to V_{cc} voltage using the sense amplifier activated by SAE signal of H. Since this read operation is destructive, the memory cell must be rewritten and the CP line is driven to L (V_{ss} voltage). Then the lines of SAE, BL and/BL, and WL are driven to L sequentially.

The hysteresis of ferroelectric memory capacitor is shown in Fig. 4. Pr is a remnant polarization and Ec is a coercive field. H_{11}/L_{11} are the states at t_{11} in Fig. 3, H_{12}/L_{12} are at t_{12}, and H_{13}/L_{13}, H_{14}/L_{14} are at t_{13}, t_{14} respectively. Bitline voltage is defined by the shape of hysteresis loop and bitline parasitic capacitance. The slopes of straight line in Fig. 4 indicate bitline capacitance. When CP is driven to H, V_{cc} voltage is applied to $C_s + C_b$ through pass transistor, where C_s is a ferroelectric memory cell capacitor and C_b is a bitline capacitance, respectively. After CP is driven to H, the ferroelectric cell capacitor is discharged and the bitline capacitor is charged. BL voltage is converged to H_{12} when the written logic state is H, and is converged to L_{12} when the written logic state is L. The large bitline voltage differences between H_{12} and L_{12} is essential for stable read operation. This read operation is referred as "cell plate step driven read scheme" (CPSD read scheme) in this paper.

The 1T/1C type memory cell is shown in Fig. 5. The difference from 2T/2C type memory cell is that the reference cell is added to each sense amplifier. In 2T/2C memory cell, the read operation is done by comparing the charge of two ferroelectric capacitors in a memory cell. However, in case of the 1T/1C memory cell, the read operation is done by comparing the

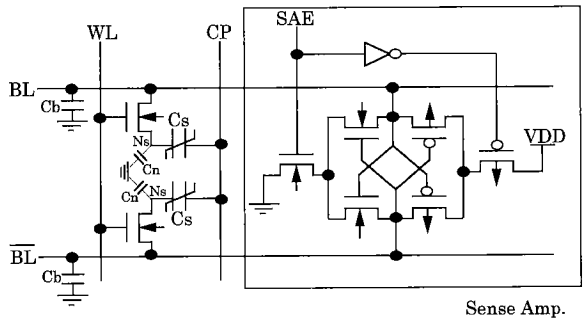

Fig. 2 2T/2C type memory cell.

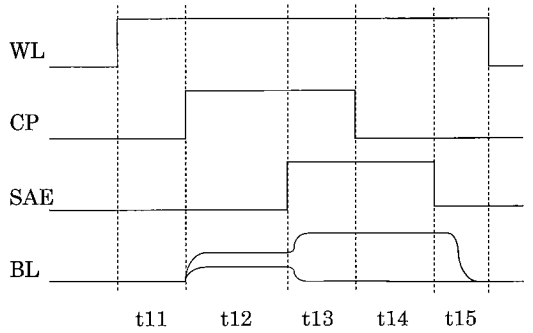

Fig. 3 The operation of CPSD read scheme.

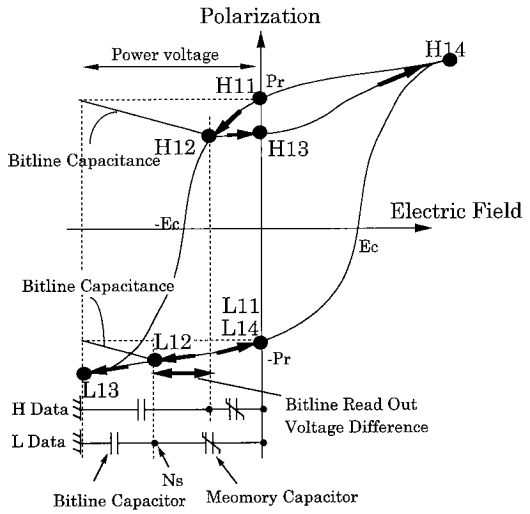

Fig. 4 The state change of ferroelectric memory capacitor with CPSD read scheme.

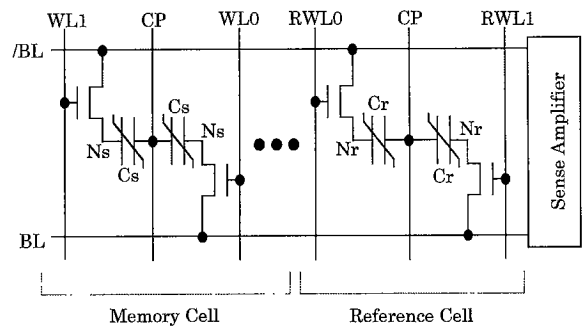

Fig. 5 1T/1C type memory cell.

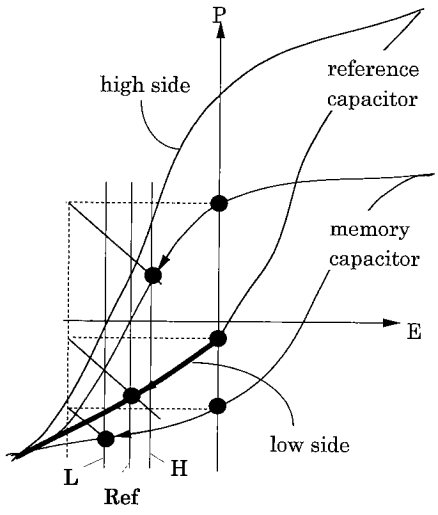

Fig. 6 Hysteresis trace of reference capacitor.

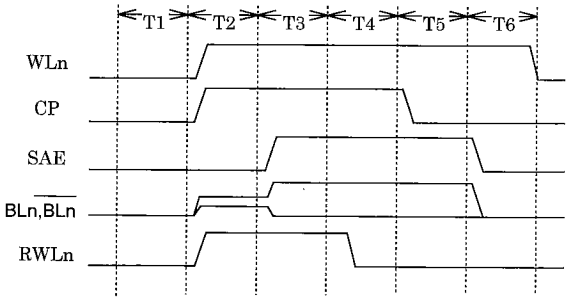

Fig. 7 Operation sequence of 1T/1C cell.

charges of memory capacitor with reference capacitor. The area of reference capacitor is several times larger than that of memory capacitor, and the reference capacitor is used in the low side of the hysteresis to generate a fixed reference level. The reference cell sets up a proper reference level automatically between level H and L at any V_{cc} voltage as shown in Fig. 6.

The read sequence is the same as the 2T/2C type memory cell, except for the reference cell (Fig. 7). It should be noted that the voltage difference between BL and/BL is the half of the voltage obtained with 2T/2C type memory cell. It means that the 1T/1C type memory cell requires more uniform and precise control of the ferroelectric memory cell capacitors than the 2T/2C type memory cell.

3. Issues of the Conventional FeRAM Circuit

The conventional circuits mentioned above have large parasitic capacitance in CP lines and are affected easily by the state of ferroelectric capacitors. Large parasitic capacitance of CP causes long operation time and high power consumption, which is a crucial problem for a practical use of FeRAM. In addition, when the circuit is in the low voltage operation, i.e. V_{cc} voltage is lower than the voltage of saturating hysteresis (about 3 V), the circuit cannot generate large voltage difference between BL and /BL at t_{12} in Fig. 3.

In a point of view of reliability, some problems also exist in the conventional circuit. One of them is the decrease of remnant polarization charge in non-selected cell capacitors while other cells are in read/write operation. In the conventional circuit, memory cells in the same column all use one CP line. As a consequence, once one of the cells is selected during the read/write operation, which means the CP is driven to H, CP of the non-selected cells in the same column are also driven to H. In turn, the storage node (Ns) of the non-selected cell is floating because WL is kept to L and the pass transistor is cut off (Fig. 2). As the Ns is floating and a parasitic capacitance (C_n) of the pass transistor is connected serially to the memory capacitor (C_s), the voltage between CP and V_{ss} are divided by C_s and C_n and the voltage of Ns is set to $V_{cc} \cdot C_s/(C_s+C_n)$. In other words, the voltage of $V_{cc} \cdot C_n/(C_s+C_n)$ is applied to non-selected memory capacitors at each read/write cycle and causes the decrease of remnant polarization charge.

The other problem is in the 1T/1C memory cell. In this configuration of Fig. 5, the reference capacitor uses only the low side of hysteresis curve and must be kept to the low side as shown in Fig. 6. If CP is driven to L while RWLn and/BL is held in H, the polarization of the reference cell is reversed. The reference cell in high side of the hysteresis loop cannot generate a correct reference voltage, and that leads to data failure. To avoid this reversal of the polarization in the reference capacitor, RWLn must be driven to L before CP is driven to L as shown in T_4 and T_5 in Fig. 7.

In spite of this operation sequence, there remains another defect. The reference level fluctuates depending upon whether the data of the memory is logic H or L. In case of the memory state in logic H, the/BL and Nr voltages are kept to V_{ss} in T_4 in Fig. 7. When CP is driven to L in T_5, Nr kept to V_{ss} in T_4 is driven to a negative voltage state. As a pn junction is formed between Nr (n^+) and the p-type substrate, Nr in T_5 is set to a built-in voltage of the junction. As a result, a negative built-in voltage remains in Cr after the read operation [2]. On the other hand, when the read out signal is logic L, any voltage, such as the built-in voltage of the pn junction, does not remain in Cr after the read operation. This fluctuation of the Cr state causes an uncertainty in the reference level and would cause a data failure.

In addition, the reference level of the circuit is easily affected by relaxation, retention, fatigue and imprint of the ferroelectric capacitors, as it is generated by the ferroelectric capacitors. These instability factors of the reference level also cause data failures in the memory, therefore the optimization of circuit parameters is necessary to achieve high reliability.

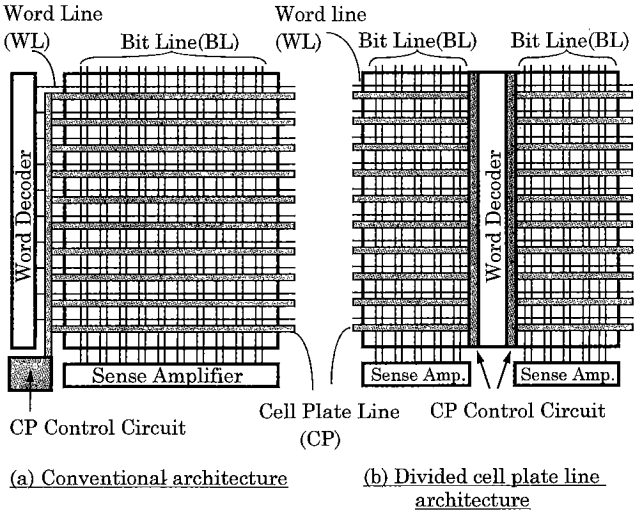

Fig. 8 Divided cell plate line architecture.

4. New Circuit Technology

4. 1 Divided Cell Plate Line Architecture

Different types of architecture for driving cell plate line (CP) are shown in Fig. 8. One is the conventional architecture that all cell plate lines in a column are connected together (Fig. 8(a)). In the other type the cell plate and its control circuit are divided by one per word line (Fig. 8(b)).

Certain issues of the conventional architecture are explained in Sect. 3:

i) long drive time and high power consumption,

ii) remnant polarization decrease in non-selected cell in read/write operation.

To avoid these problems, we adopted a new architecture in which CP is divided into one per word line as shown in Fig. 8(b). In this architecture, we can drive the memory cell separately and reduce the parasitic capacitance of CP by 77%. A drastic reduction of the current consumption from 0.52 mA to 0.12 mA is also achieved at cycle time of 200 ns in 3 V operation. Furthermore, we can achieve high reliability to avoid decreasing the remnant polarization of non-selected cell capacitors.

4. 2 Bitline High Precharged Cell Architecture

The cell plate line architecture as mentioned above is quite effective for the low power consumption, however, it needs more improvement in drive time to activate the CP signal.

Recently, another new scheme, i.e. cell plate non-driven read scheme, was proposed [3]. It is useful for high speed operation because CP line voltage is fixed at an intermediate level of supply voltage, which is about half of V_{cc}. However this scheme has two disadvantages. Since the cell plate is fixed to a half of V_{cc}, a sufficient voltage (about twice of a coercive voltage) cannot be applied to its ferroelectric capacitors, which hampers the low voltage operation. Furthermore, it requires a refresh cycle because of memory data destruction due to the leakage current from the capacitor storage node (Ns) to the substrate through a p-n junction.

To overcome these issues, we have developed a bitline high precharged read scheme as shown in Fig. 9 [4]. In this read scheme, BL are precharged to V_{cc} before the read operation, and CP is fixed to V_{ss} voltage before sense amplifier activation. The simu-

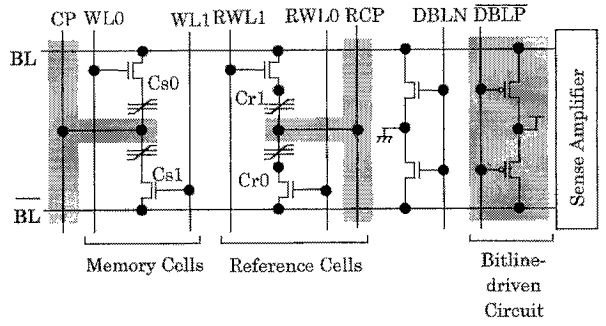

Fig. 9 Bitline high precharged cell architecture.

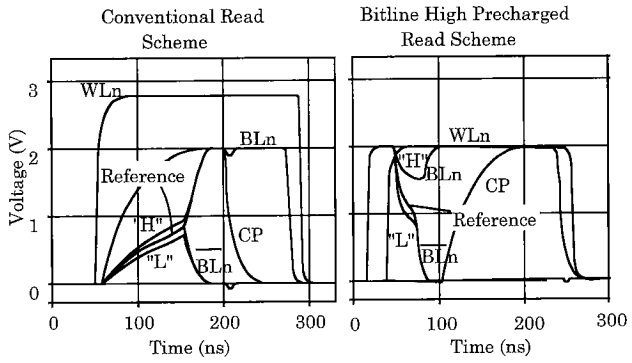

Fig. 10 Simulated waveforms of conventional read scheme and bitline high precharged read scheme.

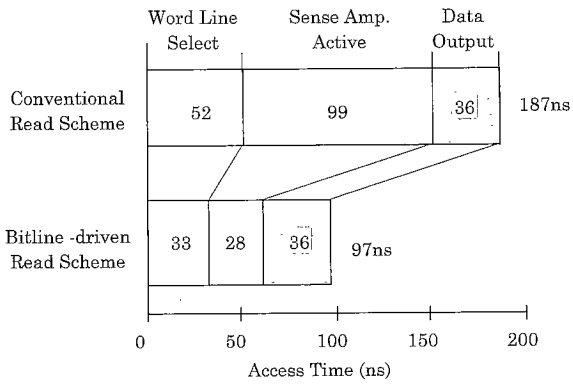

Fig. 11 The comparison of memory access time between conventional read scheme and bitline high precharged read scheme.

lated waveform of the bitline high precharged read scheme is shown in Fig. 10. For this read scheme, stored charge in ferroelectric capacitor is led to BL automatically as WL is driven to H, and a shorter access time is achieved because the data can be read before the activation of CP. After sense amplifier is activated, CP must be driven to H to rewrite memory cell capacitor. This read scheme requires no refresh cycles and achieves short access time in Fig. 11.

4. 3 Cell Plate Pulse Driven Read Scheme (CPPD Read Scheme)

Hysteresis of $SrBi_2Ta_2O_9$ gets saturated at above 3 V and the operation of the memory cell becomes stable.

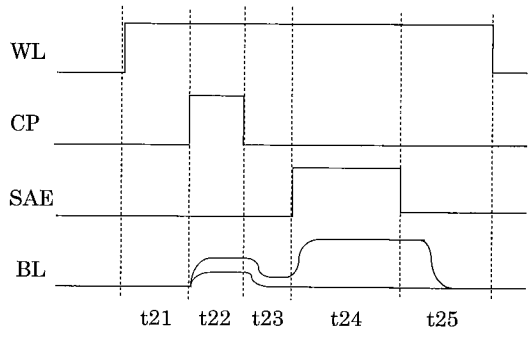

Fig. 12 The operation of CPPD read scheme.

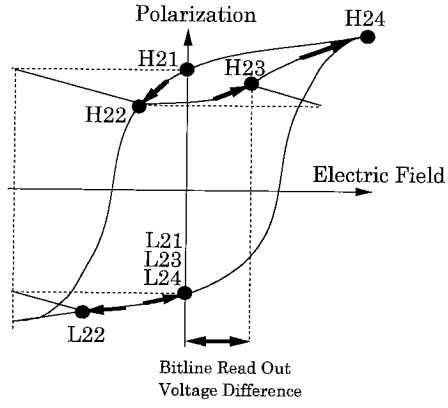

Fig. 13 The state change of ferroelectric memory capacitor with CPPD read scheme.

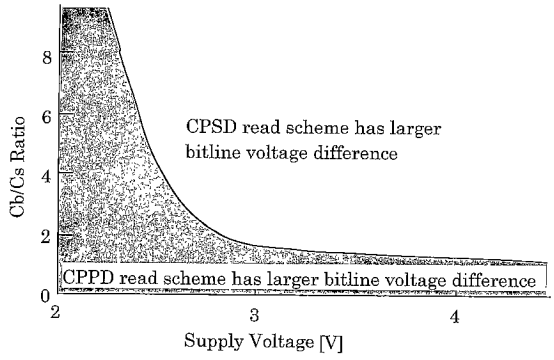

Fig. 14 The simulation result.

However, when V_{cc} voltage is low or C_b/C_s ratio is small, it does not generate a voltage difference between BL and /BL that is large enough for sense amplifier to read signals accurately. The capacitor of H state can not complete a polarization reversal because of low voltage or small C_b/C_s ratio, and the difference between the charge from H state capacitor and that from L state capacitor becomes quite small. This disturbs memory's accurate operation.

To solve this issue, we proposed cell plate pulse driven read scheme (CPPD read scheme) to achieve the stable operation at low voltage as shown in Fig. 12. In the conventional read scheme (CPSD read scheme), CP is driven to L after the activation of sense amplifier. However, in this read scheme, the CP is driven to L before the activation of sense amplifier. The state change of ferroelectric memory capacitor in CPPD read scheme is shown in Fig. 13. H_{21}/L_{21} are the states at t_{21} in Fig. 12, and H_{22}/L_{22}, H_{23}/L_{23}, H_{24}/L_{24} are the states at t_{22}, t_{23}, t_{24} respectively. The opposite side of hysterisis loop is used by driving CP to L before sense amplifier is activated. The L state trace is converged to near 0 V and the H state trace is converged to a certain positive voltage. This means that there is some difference voltage even if V_{cc} voltage is quite low. Furthermore since the BL voltage is kept low, WL need not be boosted and sense amplifier always operates at its best capability at a low voltage setting.

Figure 14 shows the result of simulation of the CPPD and the conventional CPSD read scheme. We used the model described in Ref. [5] in this simulation. This simulation model utilize the effects of space charge on the electrical properties of ferroelectric capacitor. The result of the simulation indicates that CPPD read scheme shows better characteristics than CPSD read scheme in the area of low V_{cc} voltage or small C_b/C_s ratio hatched in Fig. 14. With these backgrounds, we confirm that this read scheme is suitable for a low voltage operation, such as an embedded memory circuit of contactless IC card.

4. 4 Preset Reference Cell Architecture

In the case of 1T/1C type memory cell, it is important to generate constant reference level. In the circuit explained in Fig. 5, when the read out signal is logic L, the voltage of reference capacitor can be 0 V after the read operation, as explained in Sect. 3. Nevertheless, if the read out signal is logic H, the voltage of reference capacitor cannot be 0 V and the negative built-in voltage remains after the read operation. This means that the reference level varies depending upon whether read out signal is H or L.

To avoid the variation of the reference level, we adopted the preset reference cell shown in Fig. 15. In order to discharge the reference capacitor, an n-channel transistor is added to the conventional circuit. The

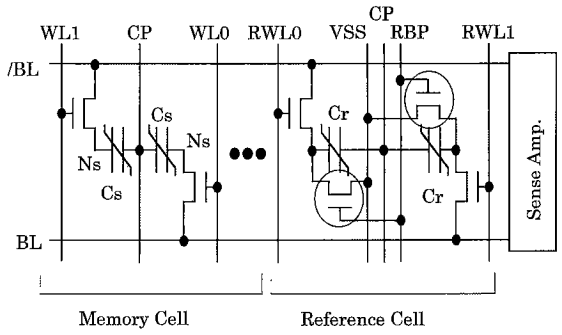

Fig. 15 Preset reference cell.

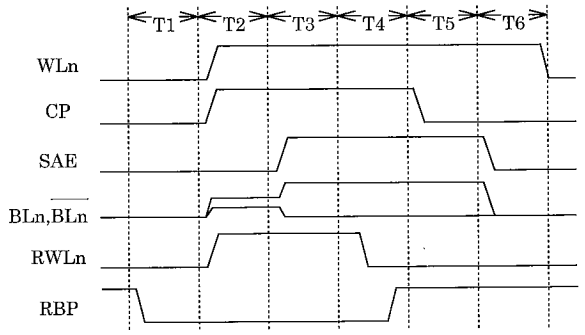

Fig. 16 Operation sequence of preset reference cell.

operation sequence is shown in Fig. 16. To keep all reference capacitors to the low side such as in Fig. 6, the RWLn of word line for reference capacitors is driven to L before CP is driven to L. The reference capacitor is set to $-V_{cc}$ voltage as RWLn and RBP to L and H, respectively, and reset to 0 V when CP is driven to L. To make reference capacitor set to $-V_{cc}$, which is the saturated voltage of hysteresis, is quite important to keep the hysteresis trace of reference capacitor constant. This reference cell architecture enables low voltage operation and high reliability because a constant reference level is generated.

4. 5 Non-relaxation Reference Cell Technology

When ferroelectric capacitor is used as a reference capacitor, the reference level is changed because the reference capacitor is also affected by relaxation, retention, fatigue and imprint. In order to avoid relaxation and retention, we proposed a non-relaxation reference cell as shown in Fig. 17 [4]. The hysteresis loop of reference capacitor is reset to the non-relaxation point after read/write operation by once being set to Vr point. This reference cell also enables low voltage operation and high reliability because it can keep the constant remnant polarization charge.

4. 6 Optimization of Read/Write Operation Time

It is important to switch the polarization of memory capacitor completely during write operation so as to

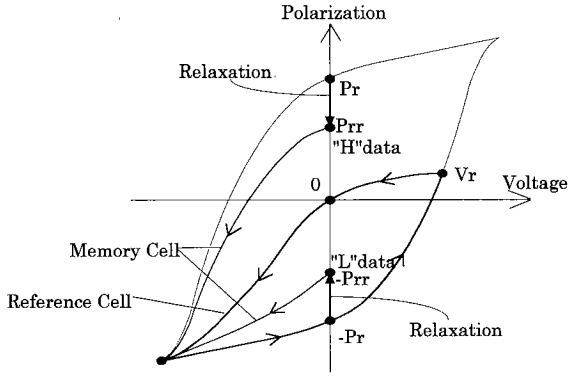

Fig. 17 Hysteresis loop trace of non-relaxation reference cell.

improve the characteristic of retention. Memory data are difficult to be written on during low voltage operation or under low temperature because hysteresis loop does not get saturated at low voltage and coercive electric field becomes large at low temperature. The conventional method we has used for simulated does not include the time response element of polarization reversal. However, the time response analysis should not be ignored when the memory operates at a high speed such as 1 MHz–10 MHz. Short write operation time prevents memorized state from reversing fully and keeps it from working properly. On the other hand, read operation time has the optimized value and read operation that's too long or short prevents proper operation. These phenomenon varies with V_{cc} voltage. We developed a simulation model [6] by measuring ferroelectric capacitor, and enabled to optimize the high speed read/write operations under various conditions. This simulation model includes time response of polarization reversal which is calculated from polarization vs. time curve of ferroelectric material and is quite similar to the actual state. A better circuit design and a high reliability are realized by this simulation.

5. Application the FeRAM Circuit Technology to LSI for Contactless IC Card

As described above, FeRAM has advanced features of high speed, low voltage write and non volatility. To utilize these features and incorporate the present circuit technology, we developed an FeRAM embedded LSI for contactless IC card (Fig. 18). The IC card which is activated by the radiation of electromagnetic field enables long operation range and high operation speed, the characteristics which has not been implemented with the conventional EEPROM technology.

The block diagram of the experimentally fabricated LSI is shown in Fig. 19. The LSI has a 5 kbit FeRAM, a 4 bit microprocessor, and an analog circuit for RF (radio frequency) communication. The specification of this LSI is shown in Table 2. The

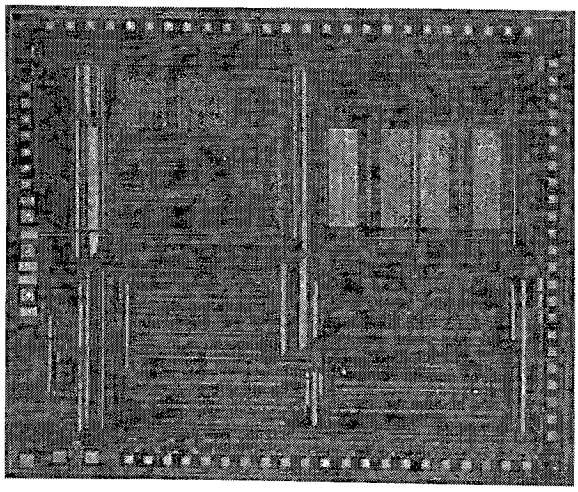

Fig. 18 The photograph of LSI for RF IC-card.

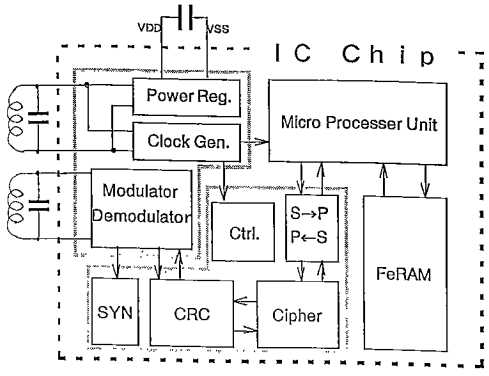

Fig. 19 The block diagram of LSI for RF IC card.

Table 2 The specification of LSI for RF IC card.

Item	Specification
IC Process	0.8 μ CMOS
MPU	4bit(MN150022)
Memory	5KbitFeRAM
Power Carrier Frequency	13.56MHz
Data Carrier Frequency	3.39MHz
MPU Clock Frequency	4.52MHz
RW→Card(ASK)	141.25kHz
RW←Card (BPSK)	141.25kHz
Read Write Range	0~10cm
Sync Code	24bit
CRC	CRC-CCITT
Cipher	built-in

frequency of power wave is 13.56 MHz and that data wave is 3.39 MHz. High speed communication (141.25 kHz) and long communication distance (0-10 cm) is achieved owing to the FeRAM. The FeRAM also realized high data reliability with above technology under the large noise from the regulator and electro-

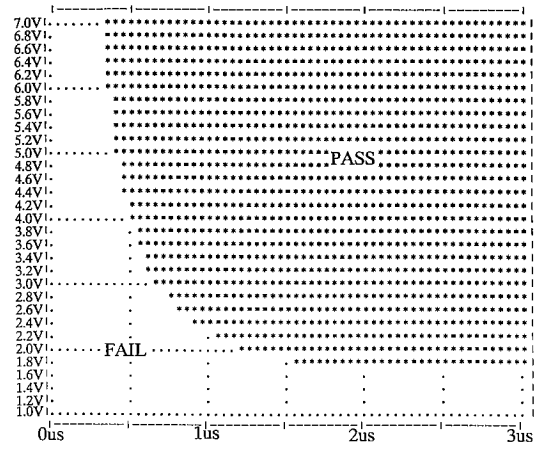

Fig. 20 Access time of 5 K FeRAM.

magnetic wave. Moreover, the FeRAM has an error correction circuit (ECC) to correct 1 bit error in 8 bit and has a screening test circuit to eliminate cells whose initial characteristics are poor. The access time vs. the V_{cc} voltage of the FeRAM is shown in Fig. 20. This memory operates even at 1.8 V V_{cc} voltage. This LSI is utilized to the electric money and commutation ticket.

6. Conclusion

We provided new circuit technology for FeRAM which is developed to implement high speed operation, low voltage operation, and low power consumption. The divided cell plate line architecture, the bitline high precharged cell architecture, and the cell plate pulse driven read scheme are demonstrated to ensure high performance. Furthermore, the reference cell technology and the optimization of read/write operation time are described as the key to obtain high reliability. The preset reference cell architecture and the non-relaxation reference cell technology are the innovations to generate constant reference level. The LSI with an implementation of above circuit technology for contactless IC card is an important application of FeRAM. This LSI is utilized to the electric money and commutation ticket.

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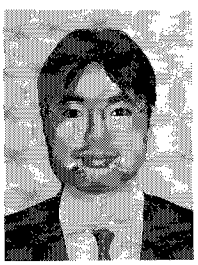
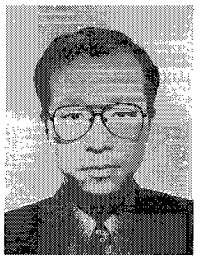
Koji Asari was born in Aichi, Japan, on June 8, 1969. He received the B.S. degree in electrical engineering from Kyoto University, Kyoto, Japan, in 1992. He joined the Electrical Research Laboratory, Matsushita Electronics Corporation, Osaka, Japan, in 1992. From 1992 to 1994, he was engaged in the design of image processor. Since 1995, he has been working on the development of ferroelectric memories.

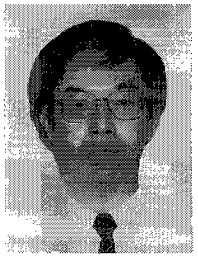


Hiroshige Hirano was born in Nara, Japan, on February 5, 1963. He received the B.S. degree in material engineering from Osaka University, Osaka, Japan, in 1985. In 1985 he joined the Kyoto Research Laboratory, Matsushita Electronics Corporation, Kyoto, Japan, where he was engaged in the design of DRAM's and embedded flash memories, and he has been working on the development of ferroelectric memories.

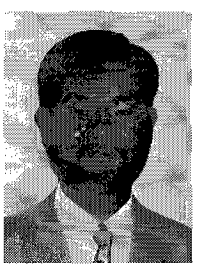
Toshiyuki Honda was born in Osaka, Japan, on February 8, 1967. He received the B.S. and M.S. degrees in electronics engineering from Okayama University, Okayama, Japan, in 1989 and 1991. In 1991 he joined Matsushita Electronics Corporation, Kyoto, Japan, where he was engaged in the design of SRAM's and embedded flash memories, and he has been engaged in the design of FeRAM's.



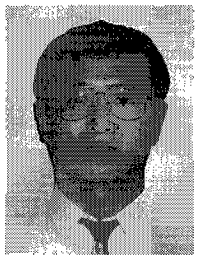
Tatsumi Sumi was born in Yamaguchi, Japan, on December 2, 1952. He received the B.S. and M.S. degrees in electrical engineering from Waseda University, Tokyo, Japan, in 1975 and 1977, respectively. In 1977 he joined Matsushita Electronics Corporation, where he worked on the design and development of bipolar analog integrated circuits. From 1981 to 1982 he was a visiting scholar of Applied Electronics Laboratory at Stanford University, Stanford, CA, where he worked on the modeling of bipolar devices. Since 1985 he has been working with Kyoto Research Laboratory, Matsushita Electronics Corporation and has been engaged in the development of advanced high-density dynamic memories. He supervised the 4 M-bit DRAM design activities. Since 1992 he has been in charge of ferroelectric device development. Currently he is a manager of IC card division at Electronics Research Laboratory. Mr. Sumi is a member of the IEEE Circuits & Systems Society. He is a co-author of books titled "Design of Semiconductor Circuits" and "Analog signal processing technology" published in Japan in 1987 and in 1991 respectively.



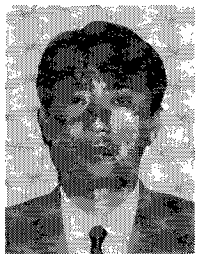
Masato Takeo was born in Mie, Japan, on December 22, 1963. He received the B.S. and M.S. degrees in nuclear technology from Osaka University, Osaka, Japan, in 1986 and 1988. In 1988 he joined the Kyoto Research Laboratory, Matsushita Electronics Corporation, Kyoto, Japan, where he was engaged in the development of evaluation technology for DRAM's and CCD's. Since 1992 he has been working on the development of evaluation technology for FeRAM's.



Nobuyuki Moriwaki was received the B.S. degree in electrical engineering from Osaka University, Osaka, Japan, in 1980. From 1980 to 1990 he was a designer of high density SRAM. In 1990 he joined Kyoto Research Laboratory, Matsushita Electronics Corporation, Kyoto, Japan, and was engaged in developing 16M-DRAM. Since 1992 he has been working on the design and development of FeRAM's.

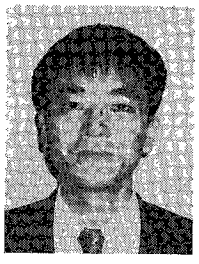


George Nakane was born in Osaka, Japan, on June 18, 1960. He received the B.S. and M.S. degrees in electronics engineering from Osaka Prefecture University, Osaka, Japan, in 1984 and 1986. In 1986 he joined Matsushita Electronics Corporation, Kyoto, Japan, where he has been engaged in the design of DRAM's and FeRAM's.

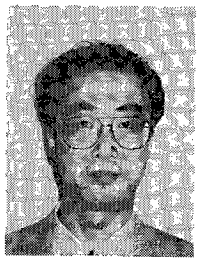


Tetsuji Nakakuma was born in Kagoshima, Japan, on January 8, 1967. He received the B.S. degree in material engineering from Kyusyu University, Fukuoka, Japan, in 1989. In 1989 he joined Matsushita Electronics Corporation, Kyoto, Japan, where he was engaged in the design of DRAM's and he has been working on the design of FeRAM's.

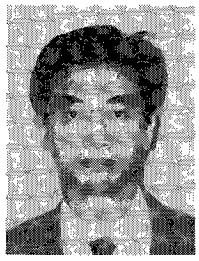
Shigeo Chaya was born in Aichi, Japan, on December 22, 1958. He received the B.S. degree in electronics engineering from Shinshu University, Nagano, Japan, in 1981. In 1981 he joined Matsushita Electronics Corporation, Kyoto, Japan, where he was engaged in the design of mask ROM's, SRAM's and embedded flash memories, and he has been working on the development of ferroelectric memories.



Toshio Mukunoki was received the B. S. degree in material science from Hiroshima University, Hiroshima, Japan, in 1991. In 1991, he joined Matsushita Electronics Corporation, Kyoto, Japan, where he was engaged in developing DRAM package. Since 1993, he has been working on the development of FeRAM.

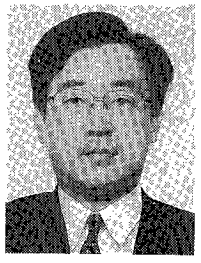


Yuji Judai was born in Osaka, Japan, on January 14, 1960. He received the B. S. and M.S. degrees in electrical engineering from Osaka University, Osaka, Japan, in 1982 and 1984. In 1984 he joined the Kyoto Research Laboratory, Matsushita Electronics Corporation, Kyoto, Japan, where he was engaged in the development of process technology for DRAM's. Since 1993 he has been working on the development of process technology for FeRAM's.



Masamichi Azuma was born in Chiba, Japan in 1959. He received an M. S. degree in material science from Tsukuba University, Ibaraki, Japan, in 1987. In 1987, he joined Matsushita Electronics Corporation, Osaka, Japan. During 1987 -1990 he worked on the CCD imager for HDTV system. Since 1991, he has been conducting research in the area of ferroelectric thin films for semiconductor integrated circuits. He is the author or co-author of several technical papers in the area of integrated ferroelectrics. He is a co-inventor in many patent disclosures in the area of ferroelectric devices for microwave applications and non-volatile memory applications. Mr. Azuma is a member of the Japan Society of Applied Physics.

Yasuhiro Shimada received the B.S. degree in physical engineering from the University of Electro-Communications, Tokyo, Japan, in 1982. He joined Matsushita, in 1982. From 1987 to 1991, he worked on R&D of excimer lasers. He is currently working for a ferroelectric device program.



Tatsuo Otsuki was born in Fukui, Japan, on August 17, 1953. He received the M.S. degree in applied physics from the University of Tokyo in 1979. In 1979, he joined the Research and Development Center of Matsushita Electronics Corporation, where he worked on development of dynamic memories. Since 1981, he has been working with Electronics Research Laboratory, Matsushita Electronics Corporation, and has been engaged in development of GaAs high speed devices. He has supervised development activities of CCD image sensors for HDTV camera system. Currently he is a manager of the advanced Si device development group at Electronics Research Laboratory.