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Voltage Shift Effect on Retention Failure in Ferroelectric Memories

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We investigated the origin of retention failure in ferroelectric memories (FeRAMs) with $SrBi_2(Ta, Nb)_2O_9$ (SBTN) memory cell capacitors by considering the time-dependent behavior of polarization vs. voltage (P-V) curves of the capacitors during high-temperature storage. Since the SBTN capacitors exhibited no marked decrease in the nonvolatile component of polarization even after high-temperature storage, we focused on the effect of voltage shift observed in P-V curves. We calculated bitline voltage along the storage from the P-V curves and the bitline capacitance, and successfully estimated a decrease in the bitline voltage, which is in agreement with the retention failure in FeRAMs. In addition, the calculation indicated that the lifetime limited by the retention failure in FeRAMs with SBTN capacitors at 125°C exceeds 10 years.

KEYWORDS: ferroelectric memory, $SrBi_2(Ta, Nb)_2O_9$, retention, voltage shif

1. Introduction

Ferroelectric memories (FeRAMs) have attracted much interest as nonvolatile memories due to their advantages in terms of high-speed and low-voltage operation while maintaining high read/write endurance exceeding 10^{12} read/write cycles.[1)] In particular, FeRAMs are in great demand for use in contactless integrated circuit (IC) card systems because of their extremely low power consumption.[2)] For the practical use of FeRAMs, however, the assessment of their nonvolatility is one of the most crucial reliability issues that must be resolved.

There are two different approaches to nonvolatility characterization: (1) statistical estimation of the retention failure in FeRAMs using a high-temperature storage test[3,4)] and (2) extrapolation of the time-dependent change in remanent polarization of ferroelectric capacitors that occurred at high temperature.[5,6)] However, the results of the two approaches hardly correlate and none of the above approaches can account for the retention failure that takes place in practical memory operation.

In this paper, we describe how the voltage shift in the polarization vs. voltage (P-V) curves of ferroelectric capacitors influences the logic sensing operation in a two-transistor and two-capacitor (2T/2C) memory cell. Considering the voltage shift in P-V curves, the minimum lifetime of FeRAMs which is limited by retention failure is estimated.

2. Experimental

2.1 Sample preparation

$SrBi_2(Ta, Nb)_2O_9$ (SBTN) capacitors were fabricated by the following process. First, SBTN thin films were prepared by a metal organic decomposition (MOD) on platinum-coated substrates. Then, platinum thin films as top electrodes were deposited on top of the SBTN thin films. The SBTN and platinum thin films were patterned by plasma etching to form SBTN capacitors, each of which had an area of 23 μm^2. Capacitor arrays consisting of 110 individual capacitors were used for the measurement of P-V characteristics. The details are described elsewhere.[7)]

2.2 Measurement

Figure 1 shows typical P-V curves, where P_s is the switched polarization obtained from a capacitor poled to positive state P_r^+ and P_{ns} is the nonswitched polarization obtained from a capacitor poled to negative state P_r^-, while a negative reading pulse was applied to the capacitors in both cases. The nonvolatile component of the polarization is defined as $P_{nv} = P_s - P_{ns}$.

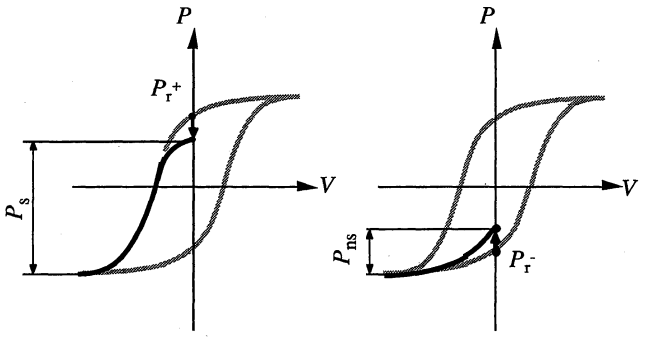

Fig. 1. P-V curves, where (a) P_s is the switched polarization obtained from a capacitor poled to a positive state P_r^+ and (b) P_{ns} is the nonswitched polarization obtained from a capacitor poled to a negative state P_r^-, while a negative reading pulse is applied to the capacitor in both cases.

For the present experiment, we performed P-V measurements in the following sequence. Prior to high-temperature stresses, ferroelectric capacitors were poled to a positive or a negative polarization state at room temperature. A Radiant Technology RT6000SI ferroelectric testing system was used for the measurement. Triangular pulses with an amplitude of ±2.7 V were used to pole the capacitors. Subsequently, the capacitors were stored at temperatures of 75°C, 100°C and 125°C from 1 to 100 h. After the storage for a specified period, triangular pulses with an amplitude of −2.7 V were applied to the capacitors at room temperature to determine the P-V characteristics. In order to avoid repetitive thermal stresses to the capacitors, different capacitors were used for each measurement.

3. Results and Discussion

3.1 Remanent polarization

Figure 2 shows retention characteristics of P_s and P_{ns} at

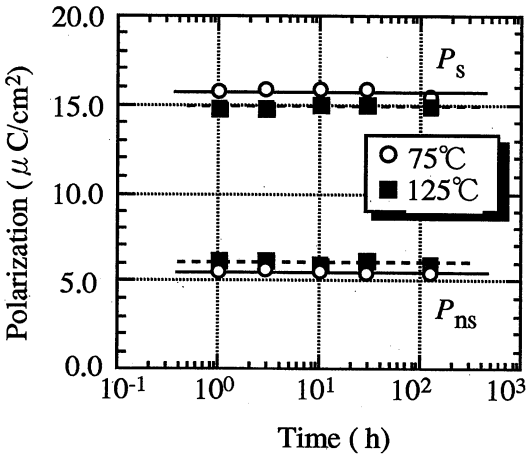

Fig. 2. Retention characteristics of P_s and P_{ns} at storage temperatures of 75°C and 125°C.

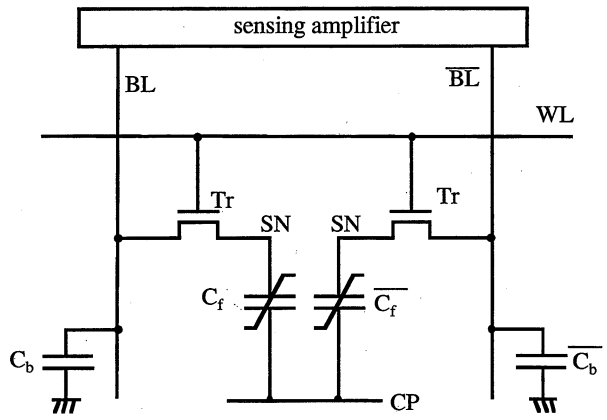

Fig. 3. Schematic diagram of a 2T/2C FeRAM cell that incorporates ferroelectric capacitors.

storage temperatures of 75°C and 125°C. Since no marked change in P_s and P_{ns} was observed in capacitors stored for 1 to 100 h, the nonvolatile component of the polarization (P_{nv}) was found to be preserved during the high-temperature storage. However, our previous work showed that the number of retention failures in FeRAMs using SBTN capacitors increases with storage time.[4] It is therefore concluded that the behavior of P_{nv} is not related to the retention failure in SBTN-integrated FeRAMs. From these considerations, we need another retention failure mechanism based on practical memory operation in FeRAMs.

3.2 *Memory operation in 2T/2C memory cell*

In an actual memory cell, it is assumed that the logic sensing operation is affected by voltage shifts in P-V curves as well as its nonvolatile components. To analyze the effect of the voltage shift in P-V curves, we chose a typical 2T/2C memory cell as described below.

Figure 3 shows a schematic diagram of a 2T/2C FeRAM cell that incorporates ferroelectric capacitors. The cell plate line (CP) corresponds to the bottom electrode of the ferroelectric capacitors, and the storage nodes (SN) to the top electrodes.

The ferroelectric capacitors (C_f and $\overline{C_f}$) are poled to opposite polarization states, and the initial voltages of the two bitlines (BL and $\overline{BL}$) are set to be zero. At the first stage of a read operation, the word line (WL) voltage is increased to reach the power supply voltage (V_{cc}) so as to connect the ferroelectric capacitor to the bitline. Then the cell plate line voltage is increased to V_{cc}. The bitline voltage is determined on the basis of the ferroelectric and bitline capacitances. When C_f is in the P_r^+ state, its polarization is reversed, while the polarization of $\overline{C_f}$ is not reversed. Consequently, the voltage at BL becomes higher than that at $\overline{BL}$, because a relatively large amount of charge is transferred to BL. The sensing amplifier determines the logic state by comparing the voltages at BL and $\overline{BL}$.

The retention failure in FeRAMs arises from the decrease in the voltage difference between BL and $\overline{BL}$ with storage time. Therefore, the investigation of the time-dependent change in the bitline voltage difference is of much importance when the retention characteristics of FeRAMs are discussed.

3.3 *Method of calculating bitline voltage from P-V curves and bitline capacitance*

The bitline voltage may change with storage time when a voltage shift in P-V curves occurs. We calculated the bitline voltage from P-V curves of ferroelectric capacitors and the bitline capacitance in FeRAMs. From the voltage relation in the memory cell during a read operation, we obtain

$$V_b + (-V_f) = V_{cc}, \tag{1}$$

where V_b is the bitline voltage, V_f (<0) is the voltage across the ferroelectric capacitor and V_{cc} is the power supply voltage. Also, from the law of conservation of charge at SN, the following equations are derived:

$$Q_b = C_b \times V_b, \tag{2}$$

and

$$Q_b + Q_f(V_f) = 0, \tag{3}$$

where C_b is the bitline capacitance, Q_b is the charge stored by the bitline capacitance and $Q_f(V_f)$ is the charge stored by the ferroelectric capacitor. By substituting eqs. (1) and (2) into eq. (3), we obtain

$$Q_f(V_f) = -C_b \times (V_{cc} + V_f). \tag{4}$$

The solution of eq. (4) can be determined by a graphical method as shown in Fig. 4. The solid curve represents $Q_f(V_f)$ in terms of the P-V curve of the ferroelectric capacitor. The straight line represents the bitline capacitance. It is therefore recognized that the bitline voltage strongly depends on the trace of the $Q_f(V_f)$ curve. Therefore, a phenomenon that changes the shape of P-V curves can affect the bitline voltage.

Warren and coworkers reported that ferroelectric capacitors, when left in a particular polarization state, exhibit voltage shifts in P-V curves.[8,9] We also observed a similar voltage shift in P-V curves of SBTN capacitors after storage at high temperature. Figure 5 shows P-V curves measured after storage times of 0.1, 1 and 100 h at 125°C. These curves exhibit considerable amounts of voltage shifts, while the retained polarizations were unchanged. When the capacitors are poled to a positive state of P_r^+, a voltage shift toward the negative voltage direction occurs during high-temperature storage.

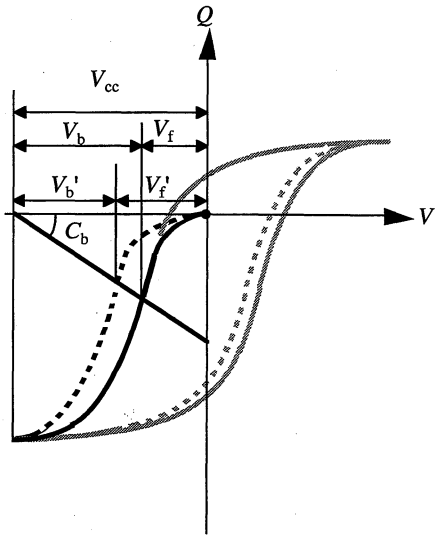

Fig. 4. *P-V* curves showing a graphical method to obtain bitline voltages.

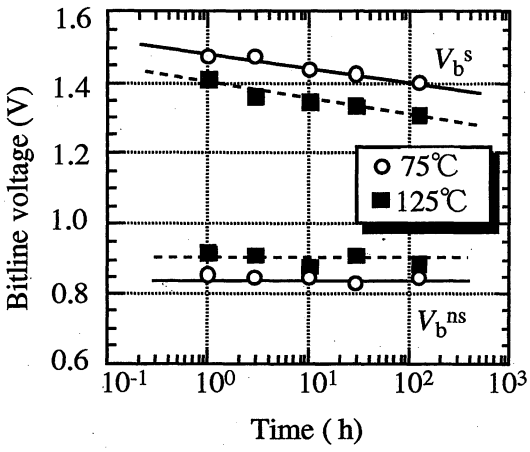

Fig. 6. Calculated bitline voltage vs. storage time. The bitline capacitance and the area of the memory capacitors are assumed to be 1.0 pF and 23 μm^2, respectively.

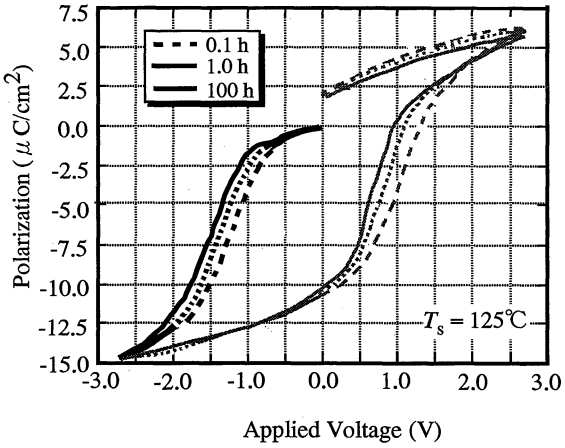

Fig. 5. *P-V* curves measured after storage times of 0.1, 1 and 100 hours at 125°C. The capacitors were poled to the positive state P_r^+ before high-temperature storage. Pulses with an amplitude of −2.7 V were used for reading.

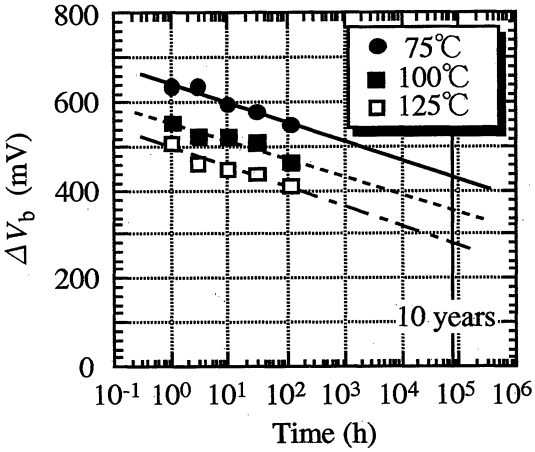

Fig. 7. Calculated bitline voltage difference ΔV_b as a function of storage time. The bitline capacitance and the area of the memory capacitors are also assumed to be 1.0 pF and 23 μm^2, respectively.

3.4 Effect of voltage shifts observed in P-V curves

Based on the above consideration, we investigated the time-dependent change in the bitline voltage caused by the voltage shifts in *P-V* curves. Figure 6 shows the bitline voltage as a function of storage time, which was calculated from the measured *P-V* curves using the graphical method. In Fig. 6, V_b^s represents the bitline voltage when the polarity of the polarization is switched, and V_b^{ns} represents the bitline voltage when the polarity of the polarization is not switched. The difference between V_b^s and V_b^{ns} is defined as ΔV_b, which represents the voltage margin for logic sensing. V_b^s exhibits a significant decrease with storage time, which is caused by a voltage shift toward the negative voltage direction. On the other hand, V_b^{ns} remains unchanged because of a small change in the *P-V* curve even if the voltage shift occurs.

Figure 7 shows the calculated bitline voltage difference ΔV_b as a function of storage time. By introducing the effect of the voltage shift in the *P-V* curves into the bitline voltage calculation, we find a decrease in the bitline voltage difference for logic sensing, which is in good agreement with the retention failure in FeRAMs. It is therefore confirmed that the voltage shift in the *P-V* curves of ferroelectric capacitors is the major cause of retention failure in practical FeRAM operation with SBTN capacitors. By extrapolating the fitting line in Fig. 7, ΔV_b after a 10-year storage at 125°C was estimated to be much larger than 200 mV, which is sufficient for logic sensing. This result proves that the SBTN capacitors have sufficient retention characteristics for application to ferroelectric memories, even when the effect of voltage shift is taken into account.

4. Conclusion

We investigated the origin of retention failure in FeRAMs with SBTN capacitors. *P-V* measurements revealed the absence of a marked decrease in the nonvolatile component of polarization, even after high-temperature storage, which implies that the nonvolatile component is not related to the retention failure in FeRAMs. We found a strong relationship between the retention failure in FeRAMs and the voltage shift in *P-V* curves of SBTN capacitors during the storage. By in-

troducing the effect of the voltage shift in P-V curves into the bitline voltage calculation, we successfully explained the decrease in the bitline voltage difference for logic sensing, which is in good agreement with the increase in retention failure of FeRAMs. It was confirmed that the voltage shift in the P-V curves of ferroelectric capacitors is the major cause of retention failure in FeRAMs with SBTN capacitors. A calculation indicated that the lifetime limited by retention failure in FeRAMs with SBTN capacitors at 125°C exceeds 10 years, which proves that SBTN capacitors have sufficient potential for practical use in FeRAMs.

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