

## Low Temperature Crystallization of SrBi<sub>2</sub>Ta<sub>2</sub>O<sub>9</sub> (SBT) Films

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(Received March 15, 2000)

650°C process of SrBi<sub>2</sub>Ta<sub>2</sub>O<sub>9</sub> (SBT) has been achieved through the use of new metal organic deposition (MOD) solution and the optimization of the deposition conditions. The sample showed a high remnant polarization (2Pr) of 14 μC/cm<sup>2</sup> @3V, a low leakage current of 10<sup>-8</sup>A/cm<sup>2</sup> or less @3V, and a fatigue-free nature. We believe this processing will realize high-density FeRAM integration of SBT.

**Keywords:** SrBi<sub>2</sub>Ta<sub>2</sub>O<sub>9</sub> (SBT); metal organic deposition (MOD); high-density FeRAM

### INTRODUCTION

SrBi<sub>2</sub>Ta<sub>2</sub>O<sub>9</sub> (SBT) is a promising material for ferroelectric non-volatile memories (FeRAMs) because of its fatigue free nature<sup>[1]</sup>. However, one disadvantage of high processing temperature of SBT is arisen as a big problem to be solved for the high-density FeRAM integration.

At present crystallization techniques, such as metal organic decomposition (MOD) etc., are commonly used for SBT film fabrication. These techniques usually require processing temperatures higher than 750°C for crystallization at thermal equilibrium to achieve good electrical properties. However, these high processing temperatures do not meet high-density CMOS LSIs with salicide contacts. Thus the lowering of processing temperature is a crucial requirement for future FeRAMs of 4M bit or higher.

Recently, K. Kato has reported lowering the process temperature of SBT using sol-gel methods<sup>[2]-[4]</sup>. She used triple alkoxide chemicals whose ion networking has similar structure to that of SBT. Using these chemicals, she reported the primary stage of crystallization of SBT is occurred above 500°C, which suggests the possibility of lowering the processing temperature of SBT. However, the electrical properties of the sample fabricated by this method at 650°C are insufficient for the actual device applications<sup>[3]</sup>.

In this paper, we will demonstrate excellent electrical properties of SBT prepared at 650°C and discuss its properties. Based on these results, we also discuss possibilities for future high-density FeRAM integration.

## EXPERIMENTAL

Table 1 shows the SBT and capacitor fabrication conditions for the experiments. The starting chemical used in this experiment is a MOD solution that involves all of the metals for SBT fabrication in one solution. This chemical was spin-coated on to the platinum (Pt) bottom electrode and pre-annealing treatments were performed subsequently. Finally, the deposited films were annealed at 650°C for 60min. for ferroelectrics phase transition. The total time of high temperature processing at 650°C is set less than 2 hours that are short enough to high density integration of FeRAMs.

For the capacitor fabrication, 200nm-thick of Pt was sputtered on to the ferroelectrics as a top electrode. The capacitor structure for the electrical measurements is Pt/SBT/Pt and its size is 6940 $\mu\text{m}^2$ . After the etching the electrode and ferroelectrics, the recovery annealing, which eliminates the damages of the ferroelectrics, was performed at 650°C for 30min.

The characterization of the deposited films was analyzed using X-ray diffraction (XRD). The incident-angle XRD measurements were performed to eliminate strong reflections from the substrate and bottom electrode. The hysteresis and fatigue properties were measured using the Sawyer-Tower method.

Table 1 Fabrication conditions and capacitor structure

Films	SrBi <sub>2</sub> Ta <sub>2</sub> O <sub>9</sub> (SBT)
Starting Solution	MOD (Metal Organic Deposition) solution
Pre-annealing	Hot Plate, Rapid Thermal Annealing (RTA), etc
Annealing Conditions	Ferro-annealing: 650°C, 60min Recovery annealing: 650°C, 30min
Capacitor structure	Pt(200nm)/SBT (100nm)/Pt(200nm) Capacitor Area: 6940 μ m <sup>2</sup>

### BASIC IDEAS FOR THE LOW TEMPERATURE PROCESSING

As an extension of existing deposition techniques, we tried to lower the processing temperature through the refinement of those deposition conditions. The optimized conditions are including starting chemicals, the furnace conditions, pre-thermal treatment conditions, etc.

Figure 1 is the schematic diagram of the free energy in SBT system. In this SBT system, a fluorite phase is existed in the low temperature range and the perovskite phase, which is possess ferroelectric properties, is considered to be high temperature phase. Even at 650°C, perovskite is stable, however, the free energy is close to that of the fluorite. Thus, the fluorite phase might be remained as a quasi-equilibrium state at 650°C<sup>[5]</sup>

The fluorite phase would be generated during heating up to 650°C and it takes more than several hours to transform from fluorite to perovskite at as low as 650°C. However, this phase transformation is easily affected by ferro-annealing conditions, the optimization of the deposition conditions, such as gas flow rate etc., can enhance this phase transformation.

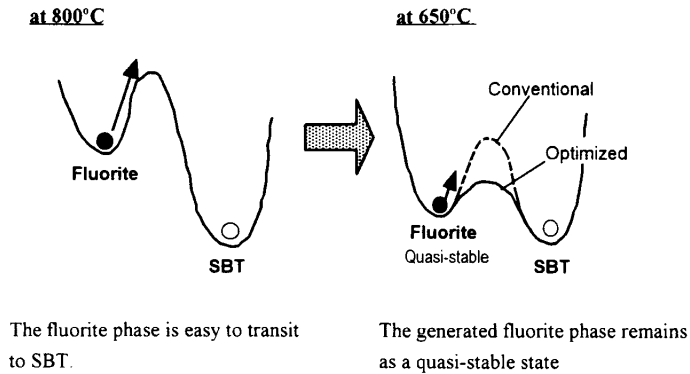


Figure 1 Schematic diagrams of the free energy of SBT system

## RESULTS AND DISCUSSION

Figure 2 shows the XRD profiles of the samples that are ferro-annealed at 650°C for 60min. The sample fabricated using conventional conditions, which is used in our present development in 800°C process, shows a single fluorite phase. In turn, the samples optimized conditions for the 650°C processing show a single perovskite phase.

Even though the same ferroannealing conditions, the results of the phase generation are completely different. As mentioned in the former section, the free energies of SBT and the fluorite phase at 650°C are close each other and this is reason that the result in fig. 2 showed opposite results even in the same ferro-annealing conditions. This result suggests that the fabrication conditions affect the SBT crystallization and optimization of the conditions is indispensable for lowering process temperatures.

Figure 3 shows electrical properties of the samples described in fig.2. As the sample fabricated in conventional conditions is the fluorite phase, it shows dielectric properties.

In turn, the sample fabricated in the optimized conditions shows good hysteresis profiles.

Its  $2Pr$  value is almost  $14\mu\text{C}/\text{cm}^2$  at 3V and it shows good saturation properties of  $2Pr$ . In addition, the sample also posses good leakage profiles that are in the order of  $10^{-8} \text{ A}/\text{cm}^2$  at 3V. (fig. 4)

These electrical properties shown in the optimized conditions are good enough for the requirements of FeRAMs, which means that this process is applicable for high-density FeRAM integration.

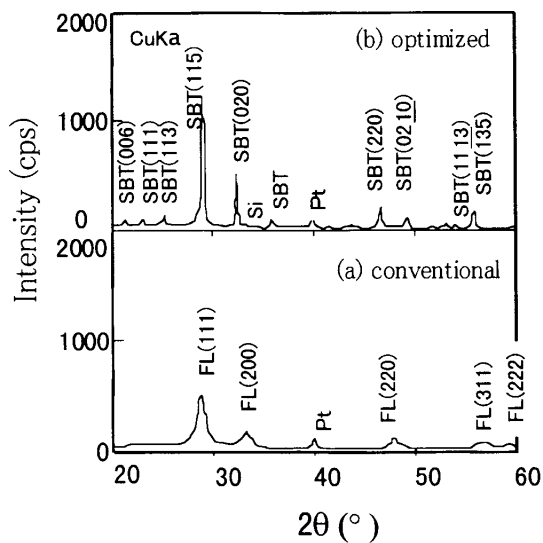


Figure 2 The XRD profiles of the samples that are fabricated in  $650^{\circ}\text{C}$  processes. The sample (a) is fabricated in the conventional conditions that are used in the  $800^{\circ}\text{C}$  process and (b) is fabricated in the optimized conditions. The characters of FL and SBT in the figure represent fluorite phase and ferroelectric phase, respectively.

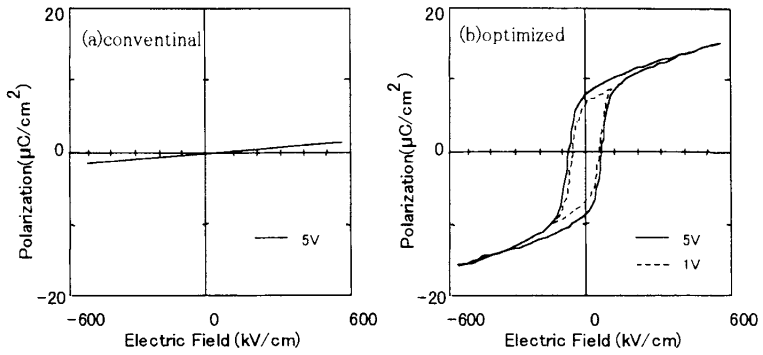


Figure 3 The hysteresis properties of the samples; (a) fabricated in conventional conditions, (b) fabricated in optimized conditions.

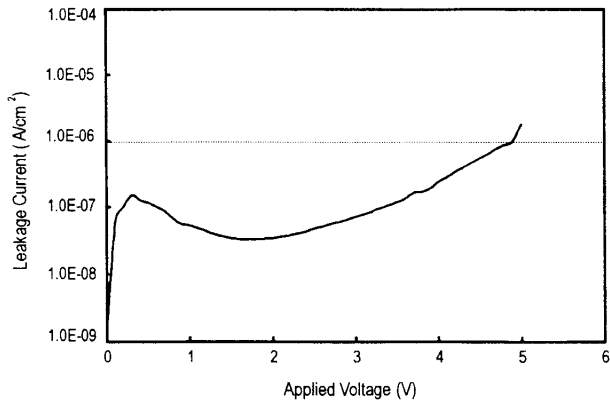


Figure 4 Leakage properties of the sample fabricated in the optimized conditions.

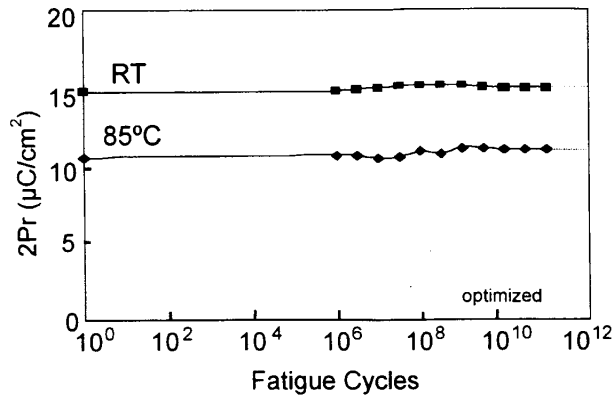


Figure 5 The fatigue measurements of the sample fabricated by the optimized conditions. The pulse used for the fatigue test was 1MHz-square and 3V. The fatigue test were performed at room temperature (RT) and at 85°C.

Finally, we will describe the fatigue properties of the sample fabricated using our low temperature processing, i.e. fabricated in the optimized conditions. The 3V-square pulse with 1MHz cycle was loaded to capacitor up to  $10^{10}$  cycles at room temperature (RT) and at 85°C. Figure 5 is the results of the fatigue measurements. Both of the measurements at RT and 85°C do not show any fatigue within the measured range. This suggests the SBT film fabricated in the low temperature processing also posses good fatigue-free nature.

As mentioned in this session, we have realized good hysteresis properties as low as 650°C ferro-annealing through the optimization of the process conditions. This result suggests that the SBT thin films are applicable for future FeRAMs with a high-density integration. We have been improving and optimizing of our processing for the mass-production applications.

### CONCLUSION

The modification and improvement of the conventional MOD method has achieved 650°C processing of SBT. The total time of high temperature processing of 650°C is less than 2 hours that is short enough for the high-density integration of FeRAMs.

The electrical properties of the sample fabricated by this process show a good hysteresis profile, a low leakage current, and a fatigue-free nature. These properties satisfy the specifications for the high-density FeRAM developments.

We believe this technique can realize the high-density FeRAMs in the near future and enlarge FeRAM markets including embedded applications.

### ACKNOWLEDGEMENTS

The authors would like to thank to Mr. Uemoto, Noma, Nasu and Tanaka of Matsushita Electronics Corporation for their support for the developments. The authors also thank to Mr. McMillan of Symetrix for his kind encouragement.

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