A Highly Reliable Ferroelectric Memory Technology with $SrBi_2Ta_2O_9$-Based Material and Metal Covering Cell Structure

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***Abstract*—A multilevel metal process-based highly reliable ferroelectric memory (FeRAM) has been developed. Highly reliable characteristics have been attained by two techniques. One is a newly developed ferroelectric material with mixed superlattice crystal of $SrBi_2(Ta_x,Nb_{1-x})_2O_9$ and $Bi_2(Ta_x,Nb_{1-x})O_6$, which provides an elevated remnant polarization while keeping a low coercive voltage. The other is a metal covering memory cell structure which makes the use of plasma silicon nitride (p-SiN) passivation possible without reduction of the ferroelectric thin film by a hydrogen plasma during p-SiN deposition, which results in no degradation of the characteristics of cell capacitors. The FeRAM cell capacitors with the above newly developed ferroelectric material and metal covering structure have been fabricated by using a 0.6-μ double level metal process. The fabricated cell capacitors show highly reliable characteristics such as the ensured retention of data written at a low voltage of 2.4 V and humidity resistance for 10 y under a high temperature of 70 °C, which is promising for commercialization of FeRAM and its embedded LSIs.**

***Index Terms*—Ferroelectric memory, multilevel, plasma silicon nitride, reliability.**

I. Introduction

FeRAM has been receiving much attention in view of its innovative features as a nonvolatile memory, such as low-voltage and high-speed read/write operation, and increased endurance cycles up to 10^{14}–10^{15} [1]–[4]. One of the most crucial issues to be solved for realizing FeRAM is to elevate its reliability characteristics to the same level as those of existing ULSIs. In particular, reliability characteristics after CMOS back-end process which includes interdielectric film deposition, contact formation, multilevel interconnect formation, and passivation should be assured because FeRAM cell capacitors are integrated with a standard CMOS logic or microcontroller unit. However, the reliability characteristics of the FeRAM fabricated using the CMOS back-end process have been less reported [5], [6], although the characteristics of the cell capacitors degrade by the reduction of the ferroelectric thin films, which is induced by the hydrogen plasma during the back-end process [7], [8].

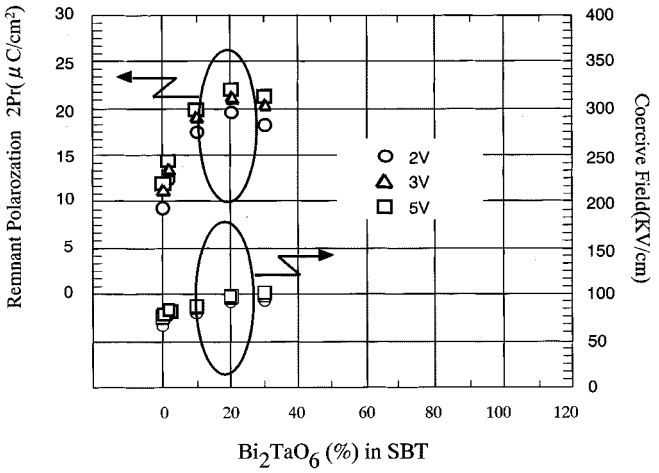

Fig. 1. Remnant polarization (2Pr) and coercive field of the mixed superlattice crystal as a function of the ratio of bismuth tantalate, which are measured just after the top electrode definition with the area of 10 000 $(100 \times 100)\,\mu m^2$.

In this paper, we demonstrate a multilevel metal process-based highly reliable FeRAM which ensures retention of data written at a low voltage of 2.4 V and humidity resistance for 10 y even under a high temperature of 70 °C for the first time [9]. These highly reliable characteristics of FeRAM are attained by the following two techniques:

1) A newly developed $SrBi_2Ta_2O_9$(SBT)-based ferroelectric material with mixed superlattice crystal of $SrBi_2(Ta_x,Nb_{1-x})_2O_9$ and $Bi_2(Ta_x,Nb_{1-x})O_6$, which provides an elevated remnant polarization while keeping a low coercive voltage.
2) A metal covering memory cell structure which makes the use of p-SiN passivation possible without reduction of the ferroelectric thin film by the hydrogen plasma during p-SiN deposition.

The first one supports 10 y retention even in the case that data is written at a low voltage of 2.4 V because the capacitors using this newly developed material have a high remnant polarization (2Pr) of 14 $\mu C/cm^2$ at a voltage of 2.4 V. The second one supports the elimination of the degradation of the characteristics of the capacitors by a p-SiN passivation process, resulting in 10 y retention and the humidity resistance at a high temperature of 70 °C.

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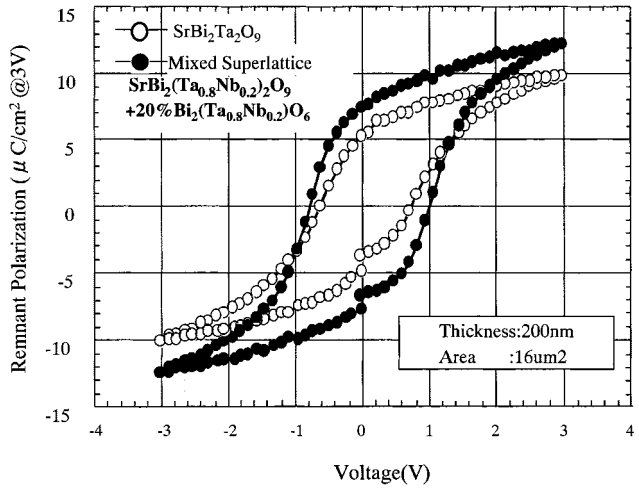

Fig. 2. Hysteresis curves of the capacitors with the mixed superlattice crystal under the supply voltage of 3 V, which are measured after the first metal interconnection.

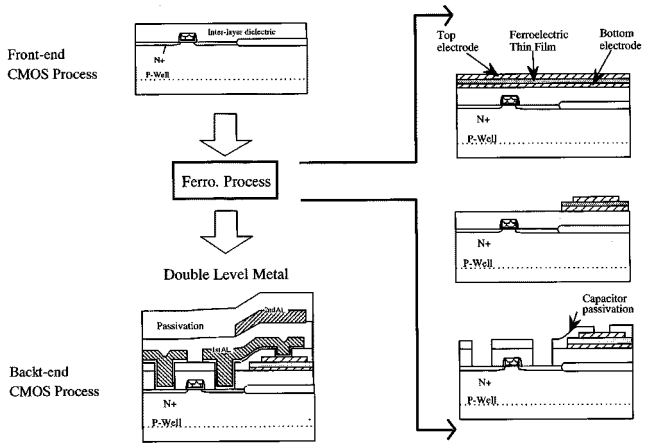

Fig. 3. Schematic cross-sectional view of the FeRAM process.

II. Results and Discussion

A. SBT-based Mixed Superlattice Crystal

It is known that the basic lattice structure of an SBT-based material consists of quasi-perovskite layers separated at periodic intervals by bismuth oxide layers [1]. The feature of this structure is that the ferroelectric characteristics such as a remnant polarization and a coercive voltage are controlled by a cation such as Ta ion, which are placed in the octahedral center, and a distance between bismuth oxide layers. In order to ensure the retention of data written even at a low voltage, a remnant polarization should be increased as large as possible while keeping a low coercive voltage. It is well known that the remnant polarization of SBT is increased by the replacement of Ta with Nb [11], [12]. However, the coercive voltage increases with increased Nb substitution, resulting in poor retention when data is written at a low voltage.

In order to overcome the above-mentioned problem, we have developed a mixed superlattice crystal of $SrBi_2(Ta_xNb_{1-x})_2O_9$(SBTN) and $Bi_2(Ta_xNb_{1-x})O_6$(BTN), which means that Ta cations are replaced by Nb and the distance between the bismuth oxide layers are changed by adding the

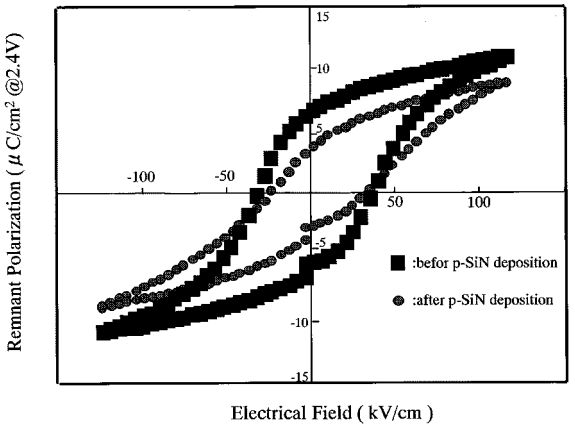

Fig. 4. Hysteresis curves of the memory cell capacitors before p-SiN deposition (■) and after p-SiN deposition (•) under the supply voltage of 2.4 V. The film thickness and capacitor area are 200 nm and 9 μm^2, respectively.

BTN to SBTN. The characteristics of the mixed superlattice crystal as a function of the ratio of bismuth tantalate to SBT are shown in Fig. 1. It is seen that the remnant polarization (2Pr) increases with increased bismuth tantalate ratio and coercive voltage remains low. The hysteresis curves of the mixed superlattice crystal of $SrBi_2(Ta_{0.8}Nb_{0.2})_2O_9$ + 20% $Bi_2(Ta_{0.8}Nb_{0.2})O_6$ with a film thickness of 200 nm and a capacitor area of 16 μm^2 are shown in Fig. 2, where those of the conventional SBT are compared. As shown in Fig. 2, the remnant polarization (2Pr) of the mixed superlattice crystal reaches almost 14 $\mu C/cm^2$, which is higher than that of the conventional SBT. It should be noted that the coercive voltages (2Vc) of the mixed superlattice crystal and the conventional SBT are 1.8 V and 1.4 V, respectively, which are almost the same value.

B. New Structure for Making the Use of p-SiN Passivation Possible

The FeRAM has been fabricated using a 0.6-μm double level metal process as shown in Fig. 3, where the process flow is schematically illustrated. As shown in Fig. 3, the cell capacitor process is inserted between the front-end CMOS process and the back-end CMOS process including the double level metal formation and the passivation by a p-SiN film. In other words, this process is compatible with the conventional CMOS logic or microcontroller unit process.

The mixed superlattice crystal film with a thickness of 200 nm was deposited using the metal-organic-decomposition (MOD) method and the memory cell capacitor was defined using reactive ion etching (RIE) with a high-energy and a high-density ion. The bottom electrode and the top electrode consist of TiO_2(100 nm)/Pt(300 nm) and Pt(200 nm), respectively. The cell storage node was connected to the access transistor using the first metal interconnection of Ti(20 nm)/TiN(100 nm)/Al(700 nm)/TiN(40 nm) deposited by the conventional sputtering method and then an O3-TEOS was deposited as the interlayer dielectric film between the first metal and the second metal. The second metal of Ti(50 nm)/Al(800 nm)/TiN(40 nm) deposited by the conventional sputtering method was patterned and finally, a p-SiN film

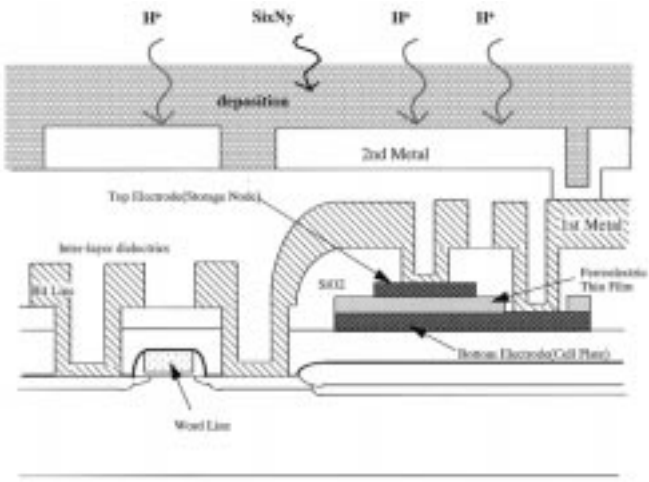

Fig. 5. Schematic cross-sectional view of the metal covering structure.

was deposited under the temperature of 400 °C and the power of 400 W as a passivation film.

It is well known that the ferroelectric thin films are easily reduced by a hydrogen plasma during p-SiN deposition, resulting in the degradation of the characteristics of the memory cell capacitors as shown in Fig. 4, where the initial hysteresis curves and those after p-SiN deposition are compared. As a result, FeRAMs developed so far have not ensured the retention of data written at a low voltage of around 3 V or has been fabricated using a silicon dioxide film as a passivation film for eliminating reduction of ferroelectric thin films. The latter means that FeRAMs are not assembled into the common plastic packages and do not ensure the humidity resistance.

In order to overcome this problem, we have developed a metal covering cell structure using the second metal of Ti(50 nm)/Al(800 nm)/TiN(40 nm) for eliminating hydrogen plasma damage during a p-SiN deposition, as shown in Fig. 5, where the cross-sectional view of this structure is schematically illustrated. As shown in Fig. 5, the second metal plays a role of a barrier layer to hydrogen plasma during a p-SiN deposition, resulting in less hydrogen damage to the ferroelectric thin films. As evidence of the effect of the barrier layer of the second metal, the remnant polarization (2Pr) of the ferroelectric capacitors have been measured by the method shown in Fig. 6, where (a) and (b) is the schematic plane view and the cross-sectional view, respectively. The measured results are shown in Fig. 7, where the barrier effect of the second metal to a hydrogen plasma during a p-SiN deposition is seen. It should be noted that no degradation of the ferroelectric characteristics is observed in the case that the edges of the second metal are arranged over those of the bottom electrode, while the ferroelectric characteristics degrade in the case of no metal covering. A cross-sectional SEM photograph of the fabricated FeRAM cell with the metal covering structure is shown in Fig. 8.

C. Reliability Characteristics of FeRAM Cell Capacitors

The retention characteristics of the fabricated cell capacitors have been measured using the procedures shown in Fig. 9, where the measurement method of the retention of the initial data and

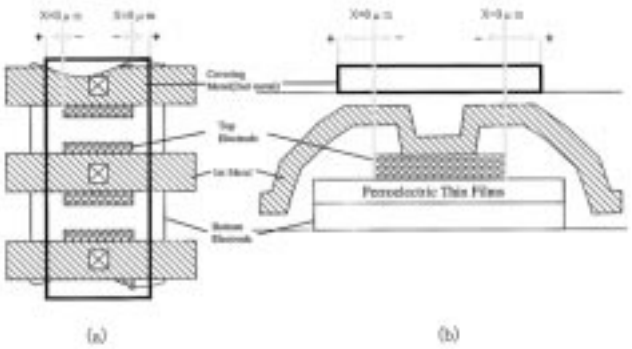

Fig. 6. (a) Schematic plane view and (b) cross-sectional view of the method for investigating the barrier effect of the second metal covering. X μm means the distance of the second metal edges from the edges of the top electrode. The film thickness and capacitor area are 200 nm and 9 (3×3) μm^2, respectively. The width of the bottom electrode is 5 μm.

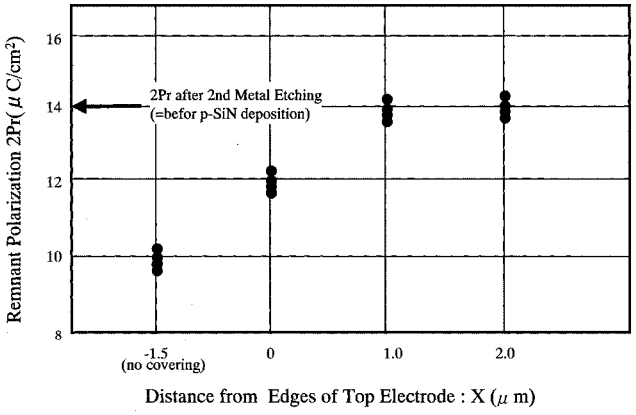

Fig. 7. Remnant polarization (2Pr) as a function of the distance (X μm) of the second metal edges from the edges of the top electrode, which is defined in Fig. 6. The supply voltage is 2.4 V. $X = -1.5$ μm means the case without the second metal covering.

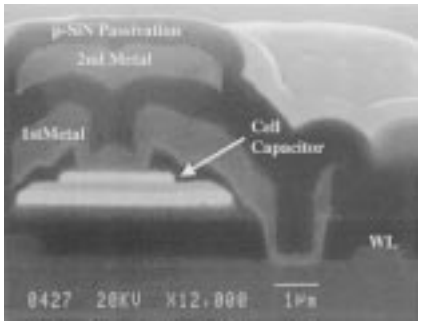

Fig. 8. Cross-sectional SEM photograph of the fabricated memory cell.

that of the opposite state to the initial state is explained [9]. The readout charge of the 2 transistors/2 capacitors(2T/2C) type of memory cell is simulated by the following method.

1) The several pairs of capacitors are provided and data of +2.4 V (write up) and that of −2.4 V (write down) are written to each capacitor.
2) The capacitors are stored for the intervals of 2 h, 20 h, and 200 h under a temperature of 125 °C. The different pairs of capacitors are used for each interval.
3) The switching charge (Qms) and nonswitching charge (Qmn) are read from the capacitors using the pulse of

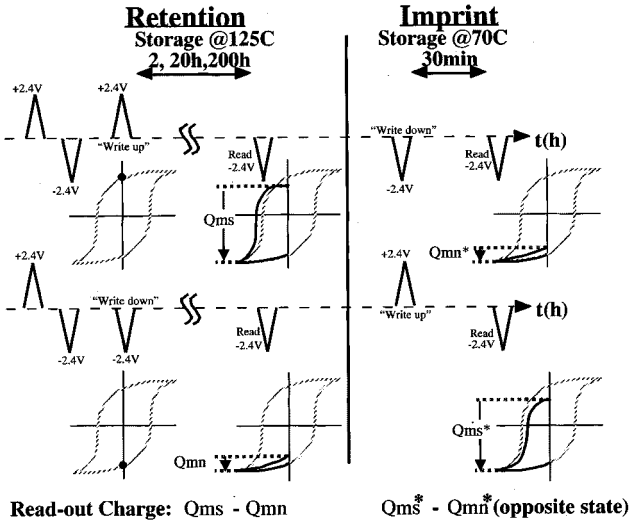

Fig. 9. Schematic view of the method for evaluating the retention characteristics of the memory cell. Retention means the charge loss of the initial data, and imprint means retention of the opposite state to the initial state, which is including the coercive voltage shift during the high temperature (125 °C) storage.

−2.4 V. The readout charge of the initial data after retention is defined as Qms-Qmn.

4) The opposite data to the initial data are written to each capacitor and the capacitors are stored at 70 °C for 30 min.
5) The switching charge (Qms*) and the nonswitching charge (Qmn*) are read from the capacitors using the pulse of −2.4 V. The readout charge of the opposite state after retention is defined as Qms*-Qmn*. This readout charge includes the imprint effect [13] caused by the coercive voltage shift during the storage at a high temperature.

The retention characteristics of the initial data and the opposite state data of the fabricated cell capacitors are shown in Fig. 10(a) and (b), respectively. As shown in Fig. 10(a), the readout charge of the initial data stays at almost initial value during time, resulting in semi-permanent retention characteristics of the fabricated cell capacitors. On the other hand, as shown in Fig. 10(b), the readout charge including imprint decreases during time. However, the readout charge stored for 10 y at 70 °C has enough margin of the minimum sensing level as shown in Fig. 10(b), where the retention time at 70 °C is estimated by the logarithmic decay model speculated from the retention model of the MNOS EEPROM [14], which is based on the existence of many dipoles in ferroelectric thin films with an energy distribution [15], [16]. In other words, the estimated retention time of the fabricated cell capacitor reaches over 10 y at a high temperature of 70 °C even when the data is written at a low voltage of 2.4 V. The excellent retention characteristics are attributed to the high-remnant polarization with a low coercive voltage of the newly developed mixed superlattice crystal and the metal covering cell structure which makes the use of p-SiN possible without the reduction of ferroelectric thin films.

The humidity resistance of the fabricated cell capacitor was evaluated using the unsaturated-pressure-cooker-test (USPCT).

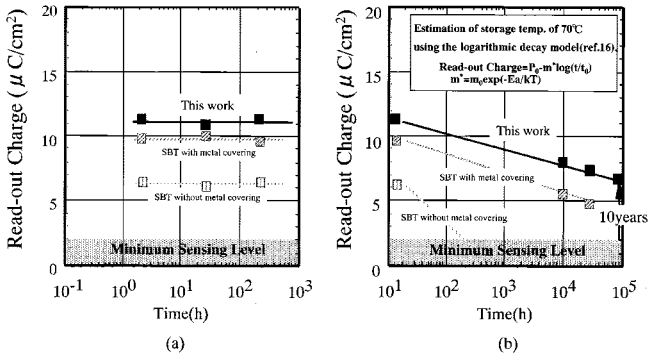

Fig. 10. Retention characteristics of (a) the initial data and (b) the opposite state to the initial state as a function of the storage time. The characteristic of the conventional SBT without metal covering (□) and the conventional SBT with metal covering (□) are also shown. The life time of 70 °C is estimated using the logarithmic decay model, which is used in the [16].

In order to apply this test, the capacitors were assembled into the conventional plastic packages and the increase of leakage currents of the capacitors were measured with time under the stress conditions of 130 °C, 85% relative humidity, and 1.4 atm. The test results are shown in Fig. 11, where (a) and (b) are the results of the capacitors fabricated using SiO_2 passivation and p-SiN passivation, respectively. The leakage currents of the capacitors fabricated using SiO_2 passivation increase with time because the electric conductance of the ceramic capacitor is very sensitive to absorption of water. On the contrary, those of the capacitors fabricated using p-SiN passivation keep the initial values because water does not diffuse into the p-SiN film. As a result, humidity resistance of 10 y is attained due to the metal covering cell structure that makes the use of p-SiN passivation possible.

III. Conclusions

We have developed the multilevel metal-based highly reliable FeRAM using the mixed superlattice crystal and the metal covering cell structure. The FeRAM fabricated using a 0.6-μm double level metal process has excellent retention characteristics and humidity resistance, which ensures retention of data written at a low voltage of 2.4 V and humidity resistance for 10 y even under a high temperature of 70 °C. These characteristics are promising for opening the door for the commercialization of FeRAM and its embedded system LSIs.

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