

LOW TEMPERATURE CRYSTALLIZATION OF MOCVD DEPOSITED SBT FILMS

K. UCHIYAMA^a, K. TANAKA^a, Y. SHIMADA^b, M. AZUMA^b, and T. OTSUKI^b,
S. NARAYAN^c, V. JOSHI^c, C. A. PAZ DE ARAUJO^c, and L. D. McMillan^c

^aPanasonic Semiconductor Development Company, 5055 Mark Dabbling Blvd.,
Colorado Springs, CO 80918, USA; ^bSemiconductor Device Research Center,
Semiconductor Company, Matsushita Electric Industrial, Co. Ltd., 1-1 Saiwai-cho,
Takatsuki, Osaka 569-1193, Japan; ^cSymetrix Corp., 5055 Mark Dabbling Blvd.,
Colorado Springs, CO 80918, USA

(Received March 14, 2001; In final form July 12, 2001)

An annealing 650°C process for SrBi₂Ta₂O₉ (SBT) has been achieved in metal organic chemical vapor deposition (MOCVD). An optimized post anneal step at 650°C is also included. The samples showed a high remnant polarization (2Pr) of 14 μC/cm² @5V, low leakage current of 10⁻⁸A/cm² or less @4V, and a fatigue-free nature. This is the first report of MOCVD deposited SBT that can achieve 650°C crystallization with the post annealing.

Key words: SrBi₂Ta₂O₉ (SBT), metal organic chemical vapor deposition (MOCVD), high-density FeRAM

INTRODUCTION

SrBi₂Ta₂O₉ (SBT) is considered to be a candidate material for ferroelectric non-volatile memories (FeRAMs) because of its high reliability nature^[1]. However, the conformal

deposition on the stepped electrodes and lowering the crystallization temperature are required to achieve high-density FeRAM integration.

At the 12th International Symposium on Integrated Ferroelectrics (ISIF'2000) in Aachen, Germany, we presented excellent conformal deposition of SBT using metal organic chemical vapor deposition (MOCVD), which is applicable for $0.18 \mu\text{m}$ (or less) rule FeRAM integrations^[2, 3].

In general, a film deposition using MOCVD is divided into two temperature regions. One is the reaction limited region that exists at relatively low temperatures and the other is the mass transport limited region that is at relatively high temperatures. Figure 1 shows deposition profiles for these deposition regions.

In the reaction limited region, the deposition rate is controlled only by the deposition temperature and is independent of MOCVD precursor supply, which is of suitable nature for the conformal deposition. However, the deposited film in this region is generally amorphous due to the low deposition temperature, i.e. 400°C , and post annealing process is needed to achieve good electrical properties.

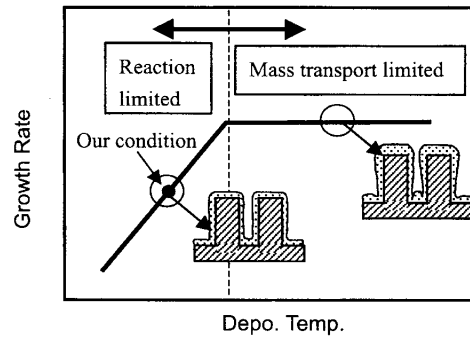


FIGURE 1 Schematics of the conformality in the MOCVD deposition

In turn, depositions in the mass transport limited region is not easy to achieve the conformality because the deposition rate is dependent on the precursor supply and the non-uniformity of the precursor delivery on to the steps will result in less conformality. Nevertheless, the deposition in this region may realize an in-situ crystallization that brings

lowering the overall crystallization temperature. Actually, M. Mitsuya et.al. have reported an in-situ crystallization as low as 585°C for $\text{SrBi}_2(\text{Ta,Nb})_2\text{O}_9$ (SBTN)^[4].

There exists a compromise of the conformality and lowering the crystallization temperature. In our former reports^[2,3], we chose deposition conditions in the reaction limited region and succeeded showing the excellent conformality on to the steps. However, because of the low temperature deposition of around 400°C, the as-deposited film is in the amorphous phase and the post annealing became a key factor for reducing the overall thermal budgets. In the former reports of MOCVD, deposited SBT films required more than 700°C post annealing temperature for crystallization^[5,6] and further lowering the post annealing temperature is required for high-density FeRAM integration.

For lowering the crystallization temperature of SBT, we have achieved and reported a specialized annealing technique with crystallization temperature as low as 650°C^[7] using samples made by metal-organic decomposition (MOD) method. We believe this technique is also applicable to the post annealing process of MOCVD and will realize both for the conformality and the low temperature crystallization.

In this paper, we demonstrate excellent electrical properties of MOCVD deposited SBT using the 650°C post annealing and discuss its properties.

EXPERIMENTAL

Table 1 shows our MOCVD deposition conditions. We used strontium tantalum methoxy-ethoxy ethoxide and triphenyl bismuth (Kojundo chemical, Japan) as the precursors for MOCVD. Both precursors are dissolved into the organic solvents and vaporized using Trijet vaporizer (Aixtron, AG, Germany) and the MOCVD deposition chamber is the Tricent system (Aixtron, AG, Germany)

As described in the introduction, we chose the lower deposition temperature around 400°C that can achieve good conformality. However, in this paper, all of the samples were deposited on to the planar platinum (Pt) electrodes to investigate just low temperature crystallization process. Conformality has been demonstrated before- and, the combinations of both conditions are in progress.

The as-deposited films are almost 200nm-thick and the average composition is Sr:Bi:Ta=0.7:2.2:2.0. (measured by X-ray fluorescent method). As-deposited SBT films

show the amorphous characteristics and post annealing processes, i.e. rapid thermal annealing (RTA) and furnace annealing (FA), are performed for the crystallization. The total thermal budget of post annealing is within 1 hour.

TABLE 1 Deposition conditions of MOCVD

MOCVD precursors	Sr-Ta: strontium tantalum methoxy-ethoxy ethoxide Bi: Tri-Phenyl Bismuth
Precursor flow	0.1 - 0.3 sccm
Film thickness	200nm
Chamber pressure	2 - 8 Torr
O ₂ flow	300 - 900 sccm
Carrier gas (Ar) flow	100 - 400 sccm
Wafer rotation	~ 10 rpm
Deposition Time	20 - 90 minutes

For the capacitor fabrication, 200nm-thick of Pt was sputtered on to the ferroelectric thin film as a top electrode. The capacitor structure for the electrical measurements is Pt/SBT/Pt and its size is 6940 μm^2 . After etching the electrode and the ferroelectric film, the recovery annealing, which eliminates the damages of the ferroelectric film, was performed at the same temperature as that of post annealing for 30 min.

Post annealing and recovery annealing conditions are summarized in Table 2. The total time of high temperature processing is set less than 2 hours. For the 650°C post annealing process, it is short enough for high-density integration of FeRAMs in the deep submicron region.

The characterization of the deposited films was analyzed using θ -2 θ X-ray diffraction (XRD) using copper K α radiation (CuK α). The hysteresis and fatigue properties were measured using the Sawyer-Tower method.

TABLE 2 Post annealing conditions and capacitor structure

MOCVD Films	SrBi ₂ Ta ₂ O ₉ (SBT) (Sr:Bi:Ta=0.7:2.2:2.0)
Deposited films	MOCVD deposited amorphous SBT
Post annealing	Rapid Thermal Annealing (RTA), Furnace Annealing (FA) etc (Total thermal budget: within 650-800°C, 1 hour)
Recovery annealing	650-800°C, 30min (same temp. as post annealing)
Capacitor structure	Pt(200nm)/SBT (200nm)/Pt(200nm) Capacitor Area: 6940 μ m ²

RESULTS AND DISCUSSION

Figure 2 (a) and (b) show the X-ray diffraction (XRD) profiles of the samples that are post-annealed at 800°C and 650°C for 1hour, respectively. Both show sharp SBT reflection peaks and no fluorite phase, though they show pyrochlore phase around 2θ=14.6°. This implies that the films processed at 650°C have almost the same crystallinity as that of 800°C.

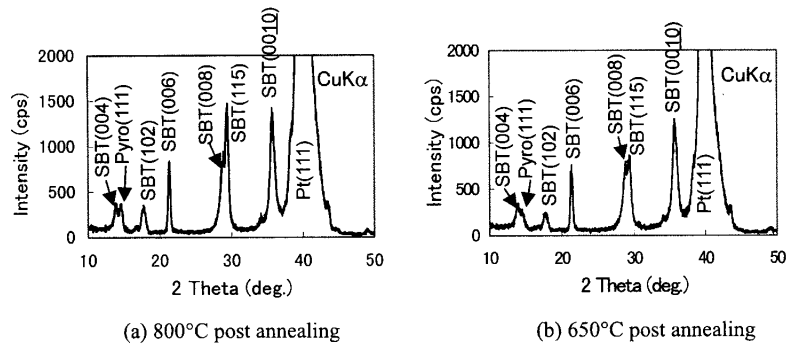


FIGURE 2 X-ray diffraction patterns after post annealing (“Pyro” in the figure means pyrochlore phase.)

If a typical non-optimized process was used, the 650°C XRD trace would show only fluorite phase. This result means that our post annealing method at 650°C is also effective in MOCVD deposited samples for lowering the crystallization temperature.

As mentioned in our former paper^[7], it is important to suppress the fluorite phase generation for lowering the crystallization temperature. Once the fluorite phase is generated, it takes long time to convert it to SBT phase. Therefore, fluorite phase skipping is a key to our post deposition annealing process.

Figure 3 (a) shows electrical properties of the sample processed at 650°C. The hysteresis loop shows as high as $14\mu\text{C}/\text{cm}^2$ of 2Pr (remnant polarization) at 5V and stable saturation features above 4V. Though the saturation voltage for this sample is slightly higher, it comes from the film thickness of 200nm and not as a result of the process scheme described above. In addition, the sample also has good leakage profiles that are in the order of $10^{-8}\text{ A}/\text{cm}^2$ at 4V. (fig. 3(b)) and do not show the breakdown up to 10V.

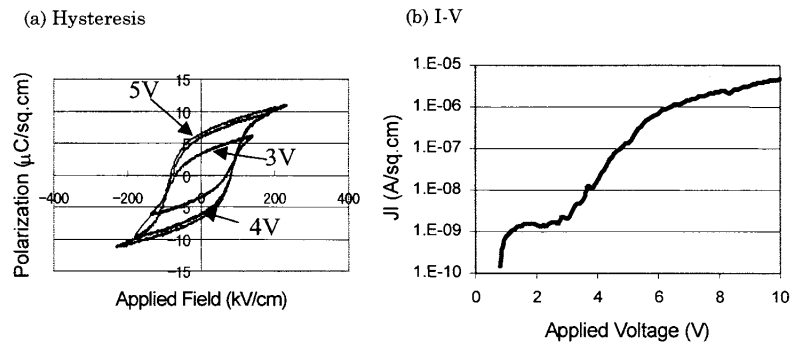


FIGURE 3 Electrical Characteristics of 200nm MOCVD deposited SBT in the low post annealing temp (650°C) region

These electrical properties show that the optimized conditions are within the expect requirements of FeRAMs, which means that this process is applicable for high-density FeRAMs.

Finally, we describe the fatigue properties of the sample fabricated using our low temperature MOCVD process. A 5V-square pulse with 1MHz cycle was applied to

capacitors up to 10^9 cycles at room temperature (RT).

Figure 4 is the results of the fatigue measurements and do not show a serious fatigue within the measured range. This suggests the SBT film fabricated by MOCVD and the low temperature post annealing also has good fatigue-free characteristics.

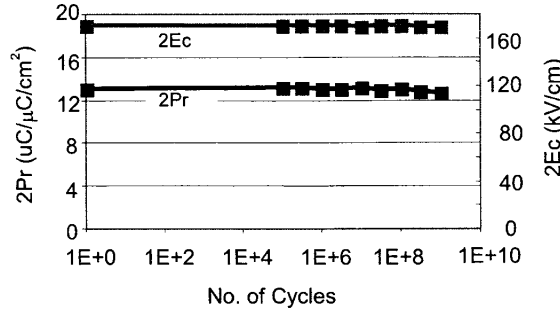


FIGURE 4 Fatigue properties of of 200nm MOCVD deposited SBT in the low post annealing temperature (650°C) region

As mentioned in this session, we have achieved device quality hysteresis properties as low as 650°C in the post annealing. This is the first report of MOCVD deposited SBT that can achieve 650°C crystallization with the post annealing. Based on this result, we have been improving and optimizing our process for mass-production applications.

CONCLUSION

We have succeeded low temperature crystallization of 650°C post annealing in MOCVD. This is the lowest crystallization of the SBT films that are deposited in the reaction limited region. We consider the results reported in this paper would achieve both for the conformality and the low temperature crystallization, which is indispensable for high-density FeRAM integration. We are investigating further optimization of the conditions and the capacitor fabrications on to the actual integrated wafers with high profile and dense

steps.

We believe this technique can realize the high-density FeRAMs in the near future and enlarge FeRAM markets including embedded applications.

ACKNOWLEDGEMENTS

The authors would like to thank to AIXTRON, AG for supporting MOCVD machine.

REFERENCES

- [1] C. A. Paz de Araujo, J. D. Cuchiaro, L.D. McMillan, M. C. Scott and J. F. Scott, *Nature*, **374**, 627 (1995).
- [2] S. Narayan, L. McMillan, C. A. Paz. de Araujo, F. Schienle, D. Burgess, J. Lindner, M. Schumacher, H. Juergensen, K. Uchiyama, and T. Otsuki, *Proc. of 12th Int. Sym. on Integr. Ferroelectr.*, Aachen, Germany (2000).
- [3] D. Burgess, F. Schienle, J. Lindner, M. Schumacher, H. Juergensen, N. Solayappan, L. McMillan, C. Paz de Araujo, K. Uchiyama, and T. Otsuki, *Jpn. J. Appl. Phys.*, **39**, 5485 (2000).
- [4] M. Mitsuya, N. Nukaga, and H. Funakubo, *Jpn. J. Appl. Phys.*, **39**, L882 (2000).
- [5] T. Eshita, H. Yamawaki, S. Miyagaki, and Y. Arimoto, *Integr. Ferroelectr.*, **26**, 805 (1999).
- [6] C. Isobe and K. Hironaka, *Proc. of 12th Int. Symp. on Integr. Ferroelectr.*, Aachen, Germany (2000).
- [7] K. Uchiyama, K. Arita, Y. Shimada, S. Hayashi, E. Fujii, T. Otsuki, N. Solayappan, V. Joshi, and C. A. Paz de Araujo, *Integr. Ferroelectr.*, **30**, 103 (2000).