0.18-μm Nondestructive Readout FeRAM Using Charge Compensation Technique

Yoshihisa Kato, *Member, IEEE*, Takayoshi Yamada, and Yasuhiro Shimada

***Abstract*—A nondestructive readout (NDRO) FeRAM using a 0.18-μm CMOS technology has been developed. Readout voltages across the ferroelectric lower than the coercive voltage allowed the FeRAM to achieve high read endurance exceeding required performance for system LSIs, 10^{16} read cycles. The NDRO approach uses a newly developed charge compensation technique to correct the process variations in threshold voltage of neighboring readout transistors, leading to a wide NDRO operation margin over a supply voltage range from 1.1 to 1.8 V.**

***Index Terms*—Ferroelectric memories, nondestructive readout.**

I. Introduction

FERROELECTRIC random access memories (FeRAMs) have remarkable advantages in low operating power, high write speed, and high write endurance over existing nonvolatile memories such as EEPROMs and Flash memories. Thanks to these superior features, FeRAMs have been implemented in remote controllers, television tuners, etc., as an alternative to EEPROMs [1], [2]. In addition, FeRAMs can be incorporated on CMOS wafers without any modifications of CMOS fabrication process and standard cell structures. We have developed a FeRAM with a memory size of 1 Mb using 0.18-μm fabrication process, which can be embedded on system LSIs [3], [4]. Smart cards incorporating the FeRAMs are opening up a new multimedia market [5]. However, for expanding the application of FeRAMs, read endurance, typically less than 10^{12} cycles, is a serious issue. In case that a FeRAM embedded system LSI operates at 100 MHz for ten years, the read endurance has to exceed 10^{16} cycles to secure the life of the FeRAM.

The limitation in read endurance results from a destructive readout operation (DRO) of FeRAMs. In the readout operation, a stored polarization is switched, so that a subsequent rewrite operation is required to restore the switched polarization [6]–[8]. As the readout operation is repeated, the polarization switching causes ferroelectric fatigue at a certain number of readout cycles, typically less than 10^{12}. In order to achieve 10^{16} cycles, a new readout operation scheme without polarization switching, nondestructive readout (NDRO) operation, is required.

Great efforts have been focused on reading the polarization without switching. For this approach, a ferroelectric gate transistor was investigated, in which a ferroelectric material is used as a gate insulator [9]–[13]. A binary datum is programmed on the ferroelectric as a polarization direction by applying a voltage between a gate electrode and a semiconductor substrate. Depending on the stored polarization direction, an inversion layer or an accumulation layer is induced on the semiconductor surface. It follows that the channel conductance changes with the stored polarization. Then, the stored datum can be read out by sensing a drain–source current with a sense amplifier in the absence of applied bias on the gate. Since no bias is applied to the ferroelectric during the readout operation, polarization switching has never occurred. For realizing the ferroelectric gate transistor, several device structures such as metal–ferroelectric–semiconductor (MFS) transistors, metal–ferroelectric–insulator–semiconductor (MFIS) transistors or metal–ferroelectric–metal–insulator–semiconductor (MFMIS) transistors have been proposed [9]–[12]. However, the ideal MFS structure is difficult to be fabricated due to an interface reaction during a high temperature growth of the ferroelectrics. On the other hand, the MFIS transistors and the MFMIS transistors have a fatal drawback in data retention limited by the presence of depolarization fields and leakage currents through the ferroelectric film. Recently, Sakai has achieved excellent data retention characteristics, the drain current ratio of the on- and off-states is more than 10^6 after 12 days, by using Pt–$SrBi_2Ta_2O_9$–Hf–Al–O–Si gate stack [13]. So, the MFIS transistor is very promising to realize high density nonvolatile memory with NDRO operation. However, this approach may extinguish the advantage of conventional FeRAMs that can be embedded on CMOS wafers without process modification, because the fabrication of the gate stack structure on CMOS wafers was not sufficiently investigated.

We have proposed a new NDRO technique which can be fabricated by using existing FeRAM process and can realize long retention time, over ten years [14], [15]. In the developed NDRO technique, a ferroelectric gate transistor is composed by connecting a gate electrode of a readout transistor and a ferroelectric capacitor. During a readout operation, small readout voltage is applied to a top electrode so as to transfer polarization charges on the ferroelectric to the gate electrode of the readout transistor, which causes slight polarization switching. Then, the stored datum is read out by sensing a drain–source current. After reading, switched polarization is automatically rewritten by removal of the readout voltage. The validity of the NDRO principle has been demonstrated with a 64-kb FeRAM which is fabricated by using 0.6-μm process.

In order to incorporate the NDRO FeRAM on the system LSIs, we have developed an advanced NDRO technique which addresses a scaling issue. Since a small amount of polarization

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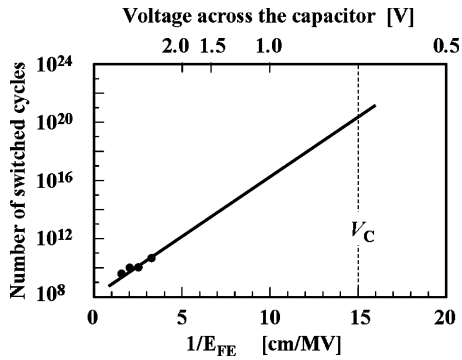

Fig. 1. Endurance cycles versus reciprocal fields.

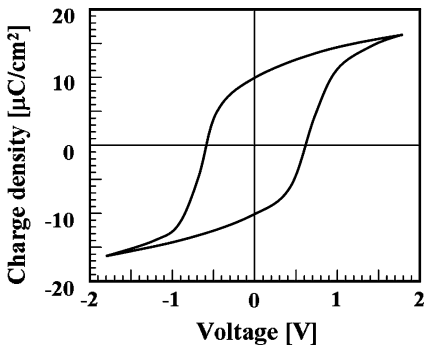

Fig. 2. Typical *Q–V* hysteresis curve of an SBT capacitor.

charges is sensed in the NDRO technique, high accuracy in performance is required to the readout transistors. However, variations of the threshold voltage (V_t) in the transistors increase along a progress of the CMOS technology [16], [17]. In this paper, we report a newly developed technique to suppress the V_t variations in the readout transistors. In addition, the validity of the advanced NDRO technique with the offset cancellation has been demonstrated with a 1-Mb NDRO FeRAM fabricated by using a 0.18-μm process [3], [4].

II. Nondestructive Readout Technique

A. Voltage Dependence of Ferroelectric Fatigue

A voltage dependence of endurance characteristics of ferroelectric capacitors fabricated by using the 0.18-μm process is shown in Fig. 1. The experimental ferroelectric capacitors were made of a $SrBi_2Ta_2O_9$ (SBT) film with platinum electrodes. The SBT films were prepared by using a metal organic deposition technique and crystallized at 800 °C by rapid thermal annealing. An average thickness of the SBT films is 100 nm and the coercive voltage V_C for this thickness is 0.6 V as shown in Fig. 2 which is a typical *Q–V* hysteresis curve.

Rectangular ac voltage pulses whose frequency is 1 kHz and duty is 50% were applied to the ferroelectric capacitors. The number of switched cycles was measured for various conditions of applied voltage, 3.0–6.0 V, which are higher than a normal operation voltage to shorten the test time. After applying a certain number of ac pulses, polarization values were measured by a Radiant RT6000SI ferroelectric test system. In order to obtain life cycles at each applied voltage, we defined them at which the measured polarizations reach a value smaller than the initial one by 10%.

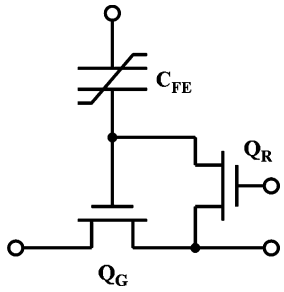

Fig. 3. Unit cell structure based on the NDRO principle.

From Fig. 1, it is found that voltage across the ferroelectrics has to be lower than 1.2 V to achieve required read endurance of 10^{16} cycles. However conventional 0.18-μm DRO FeRAMs do not meet the requirement, in which switched polarization is rewritten by applying voltage of 1.8 V after each readout operation. In order to allow such a low-voltage operation, we have developed a NDRO scheme using a unique memory cell described below.

B. NDRO Principle

Fig. 3 shows a unit memory cell circuit which is essentially a series combination of a ferroelectric capacitor $C_{\rm FE}$ and a gate capacitor C_G of a readout transistor Q_G [14], [15]. A programming voltage of 1.8 V is directly applied across the ferroelectric capacitor $C_{\rm FE}$ through a reset transistor Q_R. A binary datum of "1" or "0" is programmed on the ferroelectric capacitor $C_{\rm FE}$ in accordance with the voltage applied to both electrodes whether a voltage at a top electrode is high or low. Consequently, the polarization direction is modulated to be downward for datum "1" or upward for datum "0." After applying the programming voltage, both the capacitor electrodes are grounded. In this scheme, the polarization can be fully saturated and no bias is applied to the ferroelectric capacitor $C_{\rm FE}$ during storage period unlike the MFIS transistors or the MFMIS transistors [10]–[12]. Therefore, this NDRO technique provides a simple memory cell with long retention characteristic which can be expected to be equivalent to existing FeRAMs, over ten years.

An explanation of a NDRO scheme with a motion of the polarization on a hysteresis curve is given in Fig. 4, on which a load line of the gate capacitor of the readout transistor is overlaid. A polarization value and voltage across the ferroelectric capacitor at each stage of the readout operation described below can be obtained from the intersection of the hysteresis curve and the load line. In the NDRO scheme, the load line has a bent shape as shown in Fig. 4, since charges do not accumulated on the gate capacitor under threshold voltage V_t.

For the case of datum "1," the motion of the polarization is given in Fig. 4(a). At the first stage of reading, the reset transistor Q_R is turned off and readout voltage $V_{\rm RD}$ is applied to the top electrode. The readout voltage is divided into two components, a voltage across the ferroelectric capacitor $V_{\rm FE(1)}$ and a voltage across the gate capacitor of the readout transistor $V_{\rm FG(1)}$, determined from the ratio of their capacitance values. After reading, the top electrode is grounded keeping the reset transistor Q_R

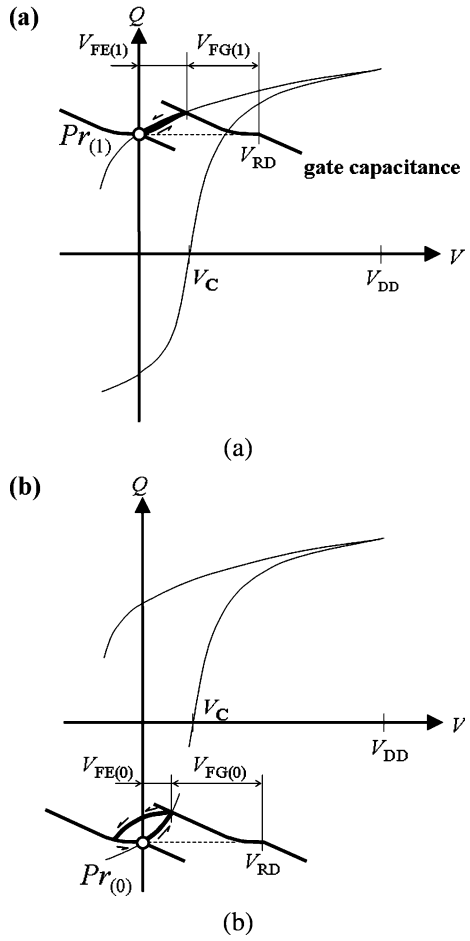

Fig. 4. Portion of a Q–V hysteresis curve overlaid with the gate capacitance. (a) Programmed datum is "1." (b) Programmed datum is "0."

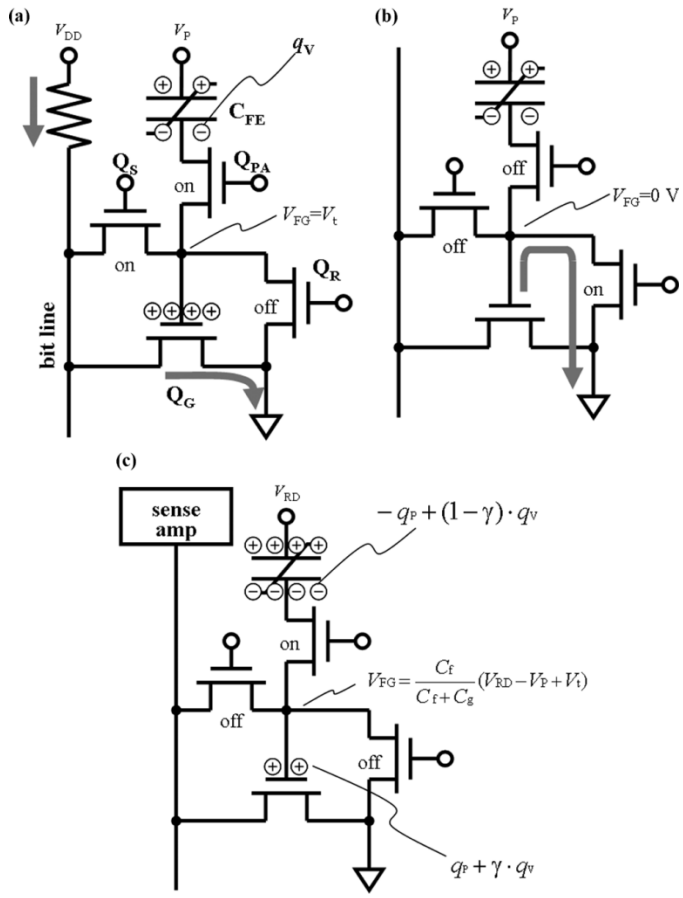

Fig. 5. Operation sequence of charge compensation sensing. (a) Charge accumulation. (b) Reset. (c) Readout.

off. In this operation, the polarization state directly goes back to the original position moving on a saturated hysteresis curve. At the end of reading, the floating gate voltage is removed by turning the reset transistor Q_R on.

For the case of datum "0," the motion of the polarization is given in Fig. 4(b). At the first stage of reading, the readout voltage is divided into two components as well as the case of datum "1" but divided voltages, $V_{\mathrm{FE}(0)}$ and $V_{\mathrm{FG}(0)}$, are different from those for datum "1" case, since the capacitance value of the ferroelectric capacitor depends on the programmed polarization. The difference in the voltage across the gate capacitor for datum "1" and "0," $V_{\mathrm{FG}(1)}$ and $V_{\mathrm{FG}(0)}$, changes the channel conductance of the readout transistor, which causes a modification of a drain–source current. Then the difference in the current is readout by using a sense amplifier. After reading, the polarization goes to a position which has the same polarization value as the original one but has negative voltage value by grounding the top electrode. At the end of reading, the polarization position completely returns to its original position by removing the floating gate voltage.

Consequently, the polarization state is read out at a low voltage without polarization flipping and returns to its original state. Therefore, the rewrite operation is not required after reading. Since the voltage across the ferroelectric capacitor during the readout operation is below the coercive voltage V_C, 0.6 V, the number of readout cycles is estimated to exceed 10^{16} cycles. Moreover, the read endurance reaches 10^{20} cycles for the case that the voltage across the ferroelectrics is set to be V_C.

C. Charge Compensation Sensing

However such a low voltage operation reduces the amount of signal charge as a tradeoff against the increased read endurance. In order to sense the small amount of charges, a memory cell is composed of two unit cells on which complementary data are programmed. Furthermore, we devised a charge compensation sensing (CCS) circuit. This circuit provides individual readout transistors with each corresponding offset compensation charge determined by individual V_t value of each transistor.

An operation sequence of CCS is as follows: For the first step [Fig. 5(a)], a pass transistor Q_{PA} turns on and both the floating gate of the readout transistor Q_G and the ferroelectric capacitor C_{FE} are connected to the bit line through a offset setup transistor Q_S, which is newly added for CCS. Then the current is flowed through the bit line and Q_G, which charges the gate capacitor of the readout transistor Q_G until the potential of the floating gate V_{FG} reaches the inherent value of V_t of the readout transistor Q_G. As a result, a V_t dependent charge $(q_V = -C_f \cdot (V_P - V_t)$, where C_f is the capacitance of the ferroelectric capacitor which is obtained from the slope of a line assuming that the hysteresis curve below the coercive voltage V_C is linear) is accumulated

on the ferroelectric capacitor as an offset charge. Meanwhile a bias voltage V_P, which is close to the coercive voltage V_C, is applied to the top electrode to prevent the polarization from being disturbed. Since the programmed polarization in the ferroelectric capacitor is nonvolatile unlike DRAMs, the polarization remains preserved even when the pass transistor $Q_{\rm PA}$ turns on to accumulate the offset charge q_V.

Following the separation of the floating gate from the ferroelectric capacitor $C_{\rm FE}$ and the bit line by turning $Q_{\rm PA}$ and Q_S off, in the second step [Fig. 5(b)], the residual charge on the floating gate is removed by turning the reset transistor Q_R on to reflect the polarization charge directly on $V_{\rm FG}$ with the offset charge.

Finally [Fig. 5(c)], Q_R is turned off and $Q_{\rm PA}$ is turned on again. Accordingly, the gate electrode of Q_G is connected with only $C_{\rm FE}$. The top electrode is pulsed to $V_{\rm RD}$ to transfer the polarization charge ($q_P = V_{\rm RD}\cdot C_f\cdot C_g/(C_f+C_g)$, where C_g is the capacitance of the readout transistor) together with a portion of q_V to the floating gate $\gamma\cdot q_V$ where $\gamma = C_g/(C_f + C_g)$. Consequently, the transferred charge $q_P+\gamma\cdot q_V$ is converted to $V_{\rm FG}$ by C_g, where $V_{\rm FG}$ is given by

$$V_{\rm FG} = \frac{C_f}{C_f + C_g}(V_{\rm RD} - V_P + V_t). \tag{1}$$

Equation (1) states that the change of $V_{\rm FG}$ caused by the V_t variation can suppress the variation of output current of the readout transistor. For example, if V_t of the readout transistor Q_G in a unit cell is higher than that in paired unit cell, $V_{\rm FG}$ is adjusted to increase the drain–source current by CCS. Consequently, even though individual V_t of each transistor deviates, the polarization charge is readout definitely by correcting $V_{\rm FG}$ automatically, which can ignore the variation in V_t.

Since the capacitance value C_f is modulated by the programmed polarization, the drain–source current depends on the datum preserved in the memory cell. By using the CCS technique, the stored datum can be read stably to sense the difference of the current.

D. Linked Cell Structure

Since the unit cell using both NDRO and CCS techniques requires more elements than conventional FeRAMs, so we devised the configuration of the memory cell to improve the area efficiency by reducing a number of elements in a cell. Fig. 6 shows a) the improved circuit configuration and b) a drive pulse sequence of a write operation and a NDRO operation which consists of a charge accumulation operation, a reset operation and a readout operation, each corresponding to Fig. 5(a)–(c), respectively. In this configuration, a unit cell consists of a pass transistor $Q_{\rm PA}$ and a ferroelectric capacitor $C_{\rm FE}$. These memory cells are linked in parallel to a readout transistor Q_G. A common read/write (r/w) circuit including the readout transistor Q_G, a reset transistor Q_R, and an offset setup transistor Q_S is shared with plural memory cells. For reading a datum stored in a certain bit of the plural memory cells, we can access it according to the former part of the pulse sequence in Fig. 6(b). For programming a datum, the bit line is connected to $C_{\rm FE}$ by turning $Q_{\rm PA}$ and Q_S on. Then the write pulse is applied to the plate line for datum "1" or the bit line for datum "0" keeping the alternative line grounded.

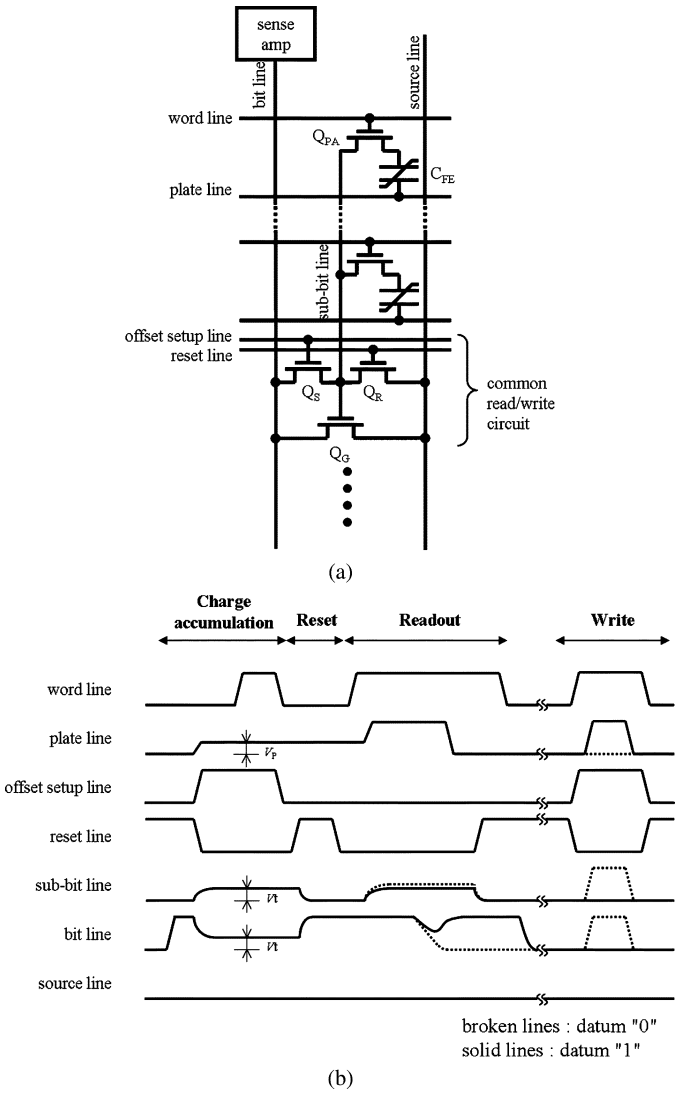

Fig. 6. Linked cell structure. (a) Circuit schematic. (b) Driving pulse sequence.

In a 0.18-μm FeRAM experimentally fabricated here, the memory cell area and the common r/w circuit are 5.2 and 5.8 μm^2, respectively. In order to make sure the relationship between the number of linked cells and the area penalty, we calculated the normalized area of the linked cell to one memory cell. Fig. 7 shows the calculation indicating that the normalized area is reduced as a number of memory cells linked to the common r/w circuit is increased. Sharing one readout transistor with more than eight cells, the increase in the area penalty will be less than 10% of the memory cell area. In addition, the linked cell structure has an advantage in relatively small capacitance of the bit line compared to that in conventional DRO FeRAM, to which few readout transistors are connected. Therefore, we can increase the number of the memory cells connected to column circuits without increasing the capacitance of the bit line. As a result, the array efficiency is improved by 35% compared to a DRO FeRAM without the linked cell structure which is designed by using the same technology.

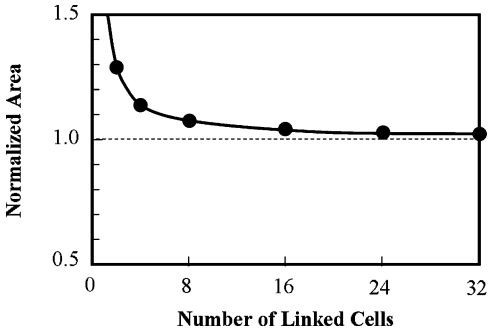

Fig. 7. Relationship between the normalized area and the number of linked cells.

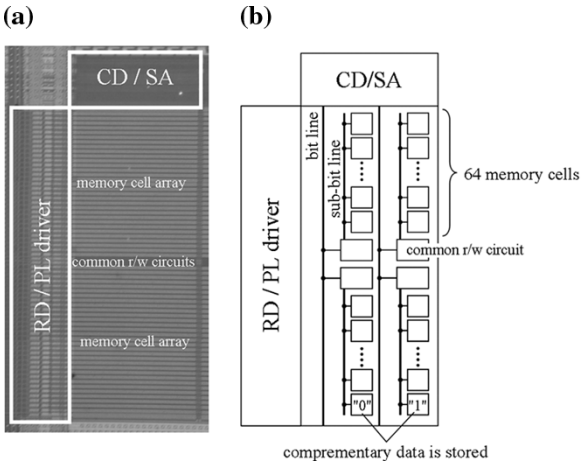

Fig. 8. One memory block in a 1-Mb NDRO FeRAM. (a) Microphotograph. (b) Block diagram.

III. Chip Performance

A. Chip Fabrication and Performance

A 1-Mb NDRO FeRAM using 0.18-μm technology [3], [4] was fabricated as shown in Fig. 8. In this FeRAM, each of 64 linked pairs of cells stores complementary data. In this memory structure, three lines arranged along column direction, bit lines, sub-bit lines and source lines, are vertically stacked in multilevel metals so that the area of a memory cell can be reduced. A column decoder circuit (CD) and a sense circuit (SA) are shared with two blocks of linked cells to improve the array efficiency. The cycle time is 350 ns at 1.8 V, which is not enough to incorporate the NDRO FeRAM on the system LSIs. So, we have already finished designing an interface circuit which is incorporated on system LSIs with the NDRO FeRAM. The interface circuit consists of two 1-kb cache memories can operate at 100 MHz.

B. Extended Readout Voltage Range

In general, the substantial increase in process variations of V_t is proportional to $1/\sqrt{LW}$, where L is a gate length and W is a gate width of a transistor [16]. In order to confirm the effectiveness of the CCS approach, readout transistors with various gate sizes were implemented on a test chip. Thus, this relationship would hold only if the CCS approach is no longer effective. Fig. 9 shows the minimum power supply voltage $V_{\mathrm{RD(min)}}$ required for reading data without error as a function of $1/\sqrt{LW}$. Without the CCS circuit, $V_{\mathrm{RD(min)}}$ increases with decreasing

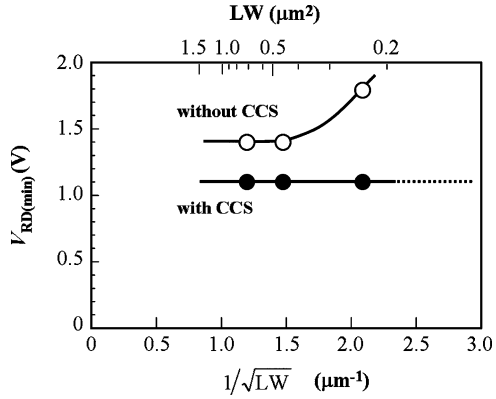

Fig. 9. Comparison of $V_{\mathrm{RD(min)}}$ for with and without CCS as a function of $1/\sqrt{LW}$.

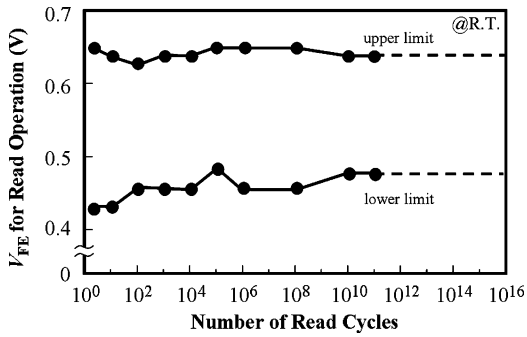

Fig. 10. Operational V_{FE} range as a function of the number of readout cycles.

the gate size and eventually reaches the power supply voltage of 1.8 V at a gate size of 0.23 μm^2 whose standard deviation of V_t mismatch in pairs was 38 mV. On the other hand, the CCS circuit can lower $V_{\mathrm{RD(min)}}$ to 1.1 V at the same gate size and is expected to be still effective for further scaling. Therefore, the NDRO operation with the CCS circuit will be available for more advanced processes below the 0.18-μm technology node.

C. Improved Reliability Characteristics of NDRO

We examined the readout endurance characteristics of the NDRO FeRAM with CCS. The memory cells of 512 bits were accessed by using the NDRO scheme and then the operational range of the power supply voltage was measured at certain numbers of readout cycles. We calculated V_{FE} from the measured power supply voltages and γ value. Fig. 10 shows the dependence of V_{FE}, corresponding to the upper and lower limit of the power supply voltage, on the number of readout cycles. The upper limit, 0.62 V, corresponds to V_C indicates that NDRO does not work properly in the voltage region where V_{FE} is larger than V_C. Under the lower limit, the polarization charge is so small that it is not enough to be readout. As shown in Fig. 10, a certain voltage margin in V_{FE} remains even after 10^{11} cycles of the NDRO operation. We believe this stable readout would continue up to 10^{16} cycles from life estimation in Fig. 1. This result indicates the validity of the newly developed NDRO technique and the availability of CCS.

In order to confirm the retention characteristic of the NDRO FeRAM, programmed data were readout after storing for 168 h at room temperature. In case of the NDRO without CCS, few

percentages of the programmed bits could not be read out correctly. We consider the reason that the NDRO scheme treats so small amount of charges compared to conventional readout method that a slight deformation of Q–V hysteresis curve make it unstable. On the other hand, most of the deteriorated bits worked well by using the NDRO with CCS. This examination indicates that the CCS technique can improve the retention characteristics of the NDRO FeRAM.

IV. Conclusion

We have established a novel nondestructive readout (NDRO) scheme that realizes high read endurance exceeding 10^{16} read cycles. A newly developed charge compensation sensing (CCS) scheme provided a stable readout operation at 1.1 V independent of the gate size by correcting the deviation in V_t of the readout transistors. A linked cell structure that can improve the area efficiency by 35% from a DRO FeRAM has been applied to a 1-Mb NDRO FeRAM using a 0.18-μm technology, which has proved the validity of CCS and the stability of NDRO after 10^{11} read cycles at 1.8 V.

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