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Improvement in Non-Destructive Readout Reliability of FeRAM with Asymmetrical Programming

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ABSTRACT

A nondestructive readout (NDRO) scheme without polarization reversal in a ferroelectric random access memory (FeRAM) is proposed as a solution for extending the number of readout cycles. However, the readout signal in an NDRO FeRAM is so small that the NDRO operation is sensitive to deformation of the $P - V$ hysteresis loop, which is a manifestation of imprint phenomena. In order to minimize the imprint effect in the NDRO FeRAM, we introduced an asymmetrical polarization programming scheme. Using this scheme, we can expect an extended number of readout cycles more than 10^{16} regardless of the imprint phenomena in ferroelectric capacitors.

Keywords: FeRAM; nondestructive readout; asymmetrical programming; imprint

I. INTRODUCTION

Ferroelectric random access memory (FeRAM) can meet the requirements for the on-chip memories integrated in a system on chip (SoC) from viewpoints of CMOS compatibility, high speed access and low voltage operation [1]. In contrast, a FeRAM has some reliability issues due to ferroelectric undesirable properties such as fatigue and imprint phenomena.

Regarding the fatigue among the properties, in the destructive readout (DRO) FeRAM, for an applied voltage across the ferroelectric capacitor (V_F^{DRO}) is higher than a coercive voltage of the ferroelectric capacitor (V_C), which is a minimum voltage to reverse the polarization, the polarization is reversed on reading. Consequently, a subsequent restore operation is necessary to rewrite the reversed polarization. Thus, since readout signal originates in the charge

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amount of remnant polarization, the readout signal decreases due to the fatigue when the readout access is repeated. As a result, the number of readout cycles is limited to approximately 10^{12}, and thus the number does not reach 10^{16} that is needed to guarantee a 10-year operation at 100 MHz, therefore, fatigue in the DRO FeRAM has been a critical issue for reliability [2].

In order to solve the fatigue issue, a nondestructive readout (NDRO) scheme has been proposed [3]. In the NDRO scheme, an applied voltage across the ferroelectric capacitor (V_F^{NDRO}) is designed to be lower than V_C, and hence the polarization is not reversed on reading. Consequently, the number of readout cycles is expected to exceed 10^{16} by minimizing the ferroelectric fatigue.

However, in the NDRO FeRAM, because the V_F^{NDRO} is lower than the V_F^{DRO}, the readout signal of the NDRO scheme is smaller than that of the DRO scheme. Accordingly, when the hysteresis loop is deformed by imprint phenomena, which is a phenomenon that a hysteresis loop is deformed at higher temperatures than a room temperature, to lower the readout signal, the NDRO scheme would readily result in a readout failure of FeRAM [4–7].

In this paper, we apply an asymmetrical program scheme to the NDRO FeRAM, which limits the deforming direction of hysteresis loop by imprint phenomena to the positive voltage direction. Therefore, the asymmetrical program scheme minimizes the imprint effect in the NDRO.

II. VOLTAGE DEPENDENCE OF ENDURANCE

We observed the voltage dependence of the endurance of polarization switching ferroelectric capacitors at 85°C as shown in Fig. 1. The Strontium Bismuth Tantalate ($SrBi_2(Ta,Nb)_2O_9$: SBT) capacitors were processed by metal organic

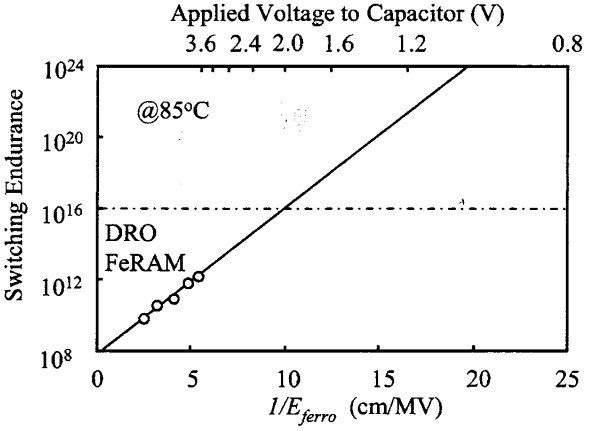

Figure 1. Switching Endurance of SBT Capacitor was measured. If the applied voltage is low enough, the switching endurance exceeds 10^{16} cycles.

deposition to have a thickness of 200 nm. We defined the ferroelectric switching endurance as the number of switching cycles when the P_r in a ferroelectric capacitor decreases 10 percents. The switching endurance increases, as the applied voltage across a ferroelectric capacitor (V_F) is lowered. However, the restoring voltage in the DRO scheme, 5.0 V, is higher than the V_C, approximately 1.7 V, and hence the restore operation causes the fatigue. Thereby, the switching endurance is limited to approximately 10^{12} or 10^{13} cycles at the restoring voltage region.

In contrast, at voltages lower than V_C, we can expect an extended endurance of more than 10^{16} cycles. From this result, if we can readout data correctly applying lower readout voltages than V_C, we can extend the readout endurance of FeRAM dramatically.

III. NONDESTRUCTIVE READOUT FeRAM WITH ASYMMETRICAL PROGRAMMING

A. Nondestructive Readout Scheme

In the DRO FeRAM, a memory cell circuit is composed of a pair of a ferroelectric capacitor and a transistor shown in Fig. 2(a). Positive remanent polarization

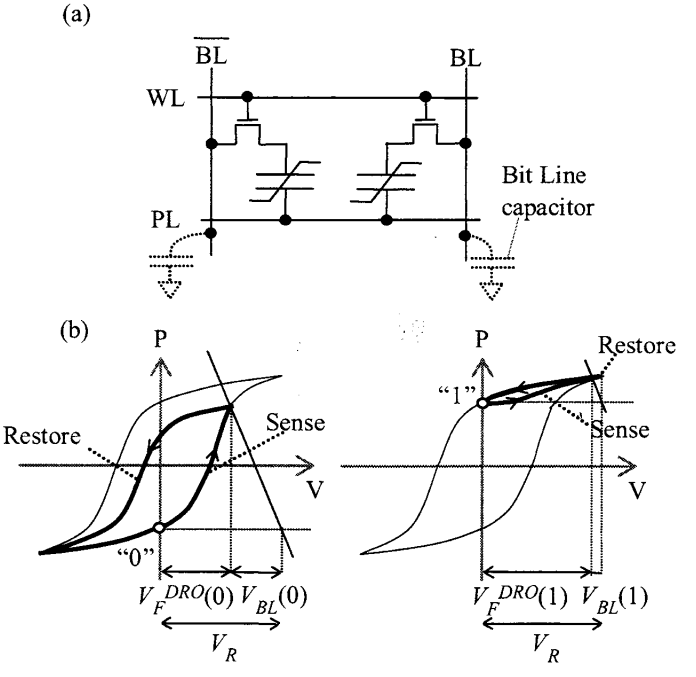

Figure 2. (a) DRO Circuit Schematic (b) Motion of Negative Polarization in DRO. It is reversed to upward every readout cycles.

(P_r^+) and negative remanent polarization (P_r^-) are assigned to a logic state of "1" and a logic state of "0," respectively as shown in Fig. 2(b).

When the logic state of "1" is read, P_r^+ is never reversed because a read voltage of V_R is positive. Then, the DRO procedure is focused and explained as follows. We define (V_F^{DRO}) (0) and (V_F^{DRO}) (1) are voltages across the ferroelectric capacitor (V_F^{DRO}) derived from data "0" and "1" relatively on reading. Firstly, a readout voltage (V_R) is applied to a plate line (PL), and thereby the V_R is divided into the (V_F^{DRO}) and the voltage across a parasitic capacitor of a bit line (V_{BL}). At the moment, since the (V_F^{DRO}) (0) reverses the negative polarization to positive polarization, the logic state of "0" is destroyed. Also, the (V_F^{DRO}) (0) and the (V_F^{DRO}) (1) indicate different voltage, because the polarization modulates the capacitance in the ferroelectric capacitor. Next, the readout signal (ΔV_F^{DRO}) between the (V_F^{DRO}) (0) and the (V_F^{DRO}) (1) is sensed. Finally, the reversed polarization is restored. Thereby, if the readout operation is repeated, this causes the fatigue. Consequently, the number of readout cycle is limited to approximately 10^{12} or 10^{13} in the DRO scheme.

To solve the fatigue issue in DRO FeRAMs, a nondestructive readout (NDRO) FeRAM has been proposed [4, 9]. Figure 3(a) shows the memory

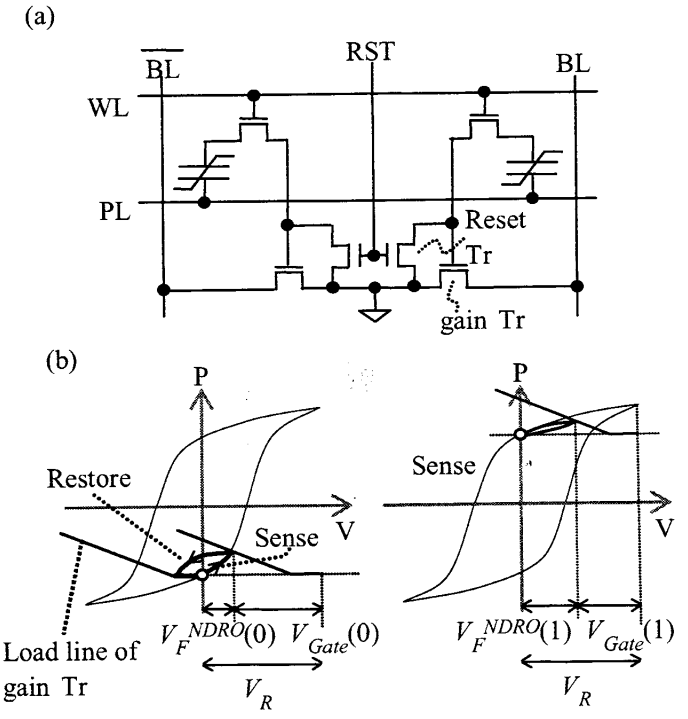

Figure 3. (a) NDRO Circuit Schematic (b) Motion of Negative Polarization in NDRO. Polarization is not reversed. Negative data is not destroyed in readout operation.

cell circuit using an NDRO FeRAM, which is composed of a pair of three transistors and a ferroelectric capacitor. Figure 3(b) shows the motion of operation point on reading using $P - V$ hysteresis loop and a load line of the gate capacitance. The shape of the load line is curved, where the inclination under the threshold voltage of the gain transistor is preferably small. As the same manner of DRO scheme, P_r^+ and P_r^- are assigned to a logic state of "1" and a logic state of "0," respectively as shown in Fig. 3(b).

The readout procedure of the NDRO is explained as follows. Firstly, a read voltage pulse of V_R is applied to PL. At this moment, the load line moves toward the positive voltage direction, and then, V_R is divided into V_F^{NDRO} and a voltage of the gate capacitor of the gain transistor (V_{Gate}). Here, V_F^{NDRO} indicates V_F^{NDRO} (0) and V_F^{NDRO} (1) in accordance with a logic state of "0" and a logic state of "1" respectively. In this circuit, V_F^{NDRO} (0) is adjusted to be lower than V_C, and hence the polarization is never reversed. Next, when the V_R is removed, the load line moves back to the original position with restoring the polarization. Thus, the NDRO scheme does not need any restore operations. Finally, to remove the electric charge accumulated at the gate of the gain transistor on reading, a reset transistor connecting ground with the gate of gain transistor is turned on to set the gate voltage grounded.

As a result, even if a small minor hysteresis loop is cycled repeatedly, the ferroelectric fatigue is never induced. Consequently, V_F^{NDRO} (0) s as small as 1.3 V under V_C, that the NDRO scheme provides a reliable FeRAM with extended readout endurance.

B. Nondestructive Readout Scheme with Asymmetrical Programming

Although the NDRO scheme is valid for extending the readout endurance of FeRAMs, the NDRO FeRAM is sensitive to the imprint effect which is an undesirable ferroelectric phenomenon that initial symmetrical hysteresis loop is deformed when the fully saturated polarization is stored for a long time under higher temperatures than room temperature. For instance, after the P_r^+ is stored for a long time under the high temperature, the hysteresis loop moves toward negative voltage direction shown in Fig. 4(a). In this case, the readout signal, ΔV_F^{NDRO}, between the V_F^{NDRO} (0) and the V_F^{NDRO} (1) increases to $\Delta V_F^{\text{NDRO-nega}}$ as the hysteresis loop moves toward negative voltage direction.

On the other hand, after P_r^- is stored for a long time at a high temperature, the hysteresis loop moves toward the positive voltage direction as shown in Fig. 4(b). In this case, the readout signal, ΔV_F^{NDRO}, between the V_F^{NDRO} (0) and the V_F^{NDRO} (1) diminishes to $\Delta V_F^{\text{NDRO-posi}}$ as the hysteresis loop moves toward the positive voltage direction.

As a result, the imprint effect toward the negative voltage direction increases ΔV_F^{NDRO}. On the contrary, the imprint effect toward the positive voltage

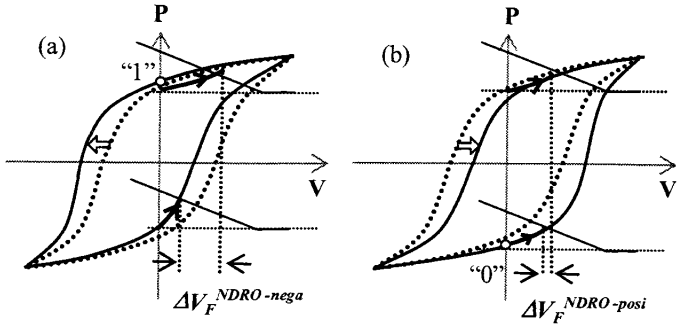

Figure 4. Symmetric NDRO FeRAM imprint effect (a) toward negative voltage direction by storing positive polarization for long time, (b) toward positive voltage direction by storing negative polarization for long time.

direction decreases ΔV_F^{NDRO}. This is a critical issue on a NDRO FeRAM because the readout signal, ΔV_F^{NDRO}, is smaller than the ΔV_F^{DRO}.

In order to suppress the imprint effect toward the positive voltage direction, we developed asymmetrical program scheme in a NDRO FeRAM. In this scheme, fully saturated positive polarization (P_r^+) and a neutral polarization are allocated to a logic state of "1" and a logic state of "0" respectively as shown in Fig. 5. Since the asymmetrical program scheme can be implemented in the cell with the same sequence of readout operation for the original NDRO FeRAM. The asymmetrical program scheme is described as follows. Firstly, a read voltage ulse of V_R is applied to PL. At this moment, the readout bit failure rate is higher than that by the original NDRO scheme, because the initial readout signal of the asymmetrical program scheme, $\Delta V_F^{NDRO\text{-}asym}$, is smaller than initial ΔV_F^{NDRO}. However, the polarization storing the logic state of "0" is not affected by the imprint effect, because the neutral polarization is not affected by

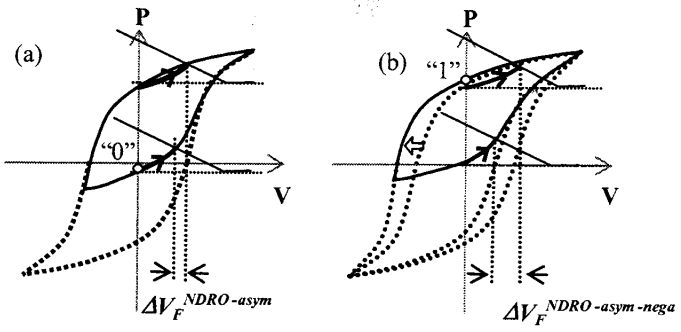

Figure 5. Asymmetric NDRO FeRAM (a) before imprint effect, (b) after imprint effect toward positive voltage direction by storing negative polarization for long time.

the imprint phenomenon. As a result, only the P_r^+ can deform by the hysteresis loop by the imprint phenomenon. Furthermore, the hysteresis deformation toward the negative voltage direction increases the readout signal from initial $\Delta V_F^{\text{NDRO-asym}}$ to $\Delta V_F^{\text{NDRO-asym-nega}}$ as shown in Fig. 5. Finally, when V_R is removed, the logic state of "0" is restored automatically as the same manner used in the original NDRO scheme. Consequently, if the NDRO FeRAM using the asymmetric program scheme is stored under high temperatures, the imprint effect does rather increases the readout signal. As a result, we can improve the readout reliability of a NDRO FeRAM using asymmetrical programming scheme.

IV. EXPERIMENTAL

In order to investigate the improved reliability of the asymmetrical program scheme, we designed and fabricated 64 K bits FeRAMs using 0.6 μm CMOS technology, whose memory cell is composed of two transistors and two capacitors, as shown in Table 1 and Fig. 6. For the presence of the overhead transistors, gain transistors and reset transistors, memory cell is larger than the conventional memory cell as shown in Fig. 3(a). To minimize the overhead of the transistors, by sharing a gain transistor with plural memory unit cells shown in Fig. 6(b), the average memory cell size can be reduced.

In the integrated FeRAM, it is impossible to measure the hysteresis loop of a ferroelectric capacitor directly. So, in order to measure the influence of the imprint effect quantitatively, we measured a minimum readout voltage (V_R^{MIN}) in the following experiments. The V_R^{MIN} is defined as the minimum voltage to readout the value stored in memory cells after some stress such as thermal stress of high temperature or voltage cycling. To decide the V_R^{MIN}, we swept the read voltage pulse of V_R from 0 V to 2.8 V increasing V_R by a step of 0.1 V. Then, when the readout signal exceeds the voltage detected by a sense amplifier integrated in the FeRAM, we defined the V_R as the V_R^{MIN}. In a practical FeRAM, values of V_R^{MIN} have statistical distribution, and hence the most important V_R^{MIN}

Table 1
Sample device features

FeRAM Size	64 K bits
Process technology	0.6 μm CMOS
Ferroelectric material	$SrBi_2(Ta,Nb)_2O_9$
Area of ferroelectric capacitor	3.0 μm × 3.0 μm
Thickness of ferroelectric capacitor	200 nm
FeRAM Configuration	2T-2C

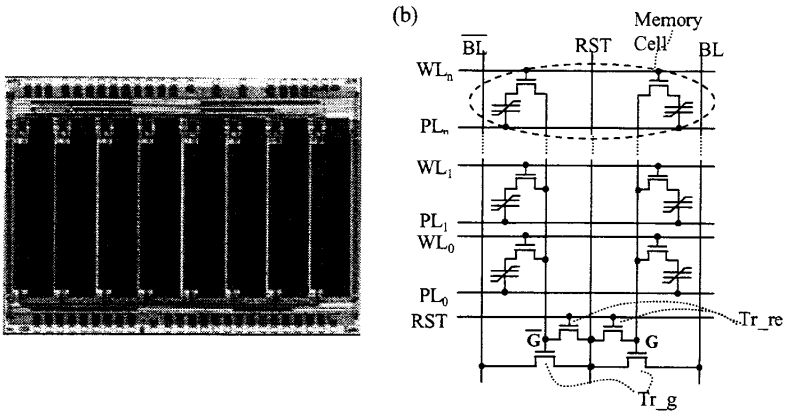

Figure 6. (a) 64 kb NDRO FeRAMs were designed and fabricated. (b) Linked Cell architecture in the experimental FeRAM is shown. Sharing the gain transistor with memory cell unit reduces average memory cell size.

is the highest value of V_R^{MIN}, because a read voltage pulse of V_R to readout all values stored in FeRAM must be a higher voltage than the highest value among all V_R^{MIN} s. Therefore, we evaluated the highest V_R^{MIN} among all V_R^{MIN} s after measuring all V_R^{MIN}.

Extended Readout Reliability of NDRO FeRAM with Asymmetrical Program Scheme

We conducted a following reliability experiment to demonstrate the improvement of the readout reliability of asymmetrical programming in NDRO FeRAMs. The readout procedure is shown in Fig. 7. Prior to readout operation, an RST is set to a high voltage to turn on Tr_re. Next, voltages of BL and BLB (V_{BL}, V_{BLB}) are pre-charged to V_{DD}. Then, a voltage of WL is supplied to a high voltage to connect a gate of gain transistor to a ferroelectric capacitor electrically. Next, PL is applied to a readout pulse voltage to recall a stored data in a ferroelectric capacitor. At that time, according to a direction of polarization, the voltage of a gate of gain transistor is different. After that, because the channel resistance of the gain transistor is different due to the voltage of gate of a gain transistor, charge amount at BL is different. After that, sensing amplifier connected to BL is turned on, so the BL voltage is amplified.

The NDRO FeRAMs were programmed using both symmetrical and asymmetrical programming. The voltage required for programming a positively saturated polarization was 5.0 V and the voltage required for programming a polarization at the neutral position is −2.8 V. Secondly, these FeRAMs were exposed under a high temperature of 125°C to accelerate the imprint effect.

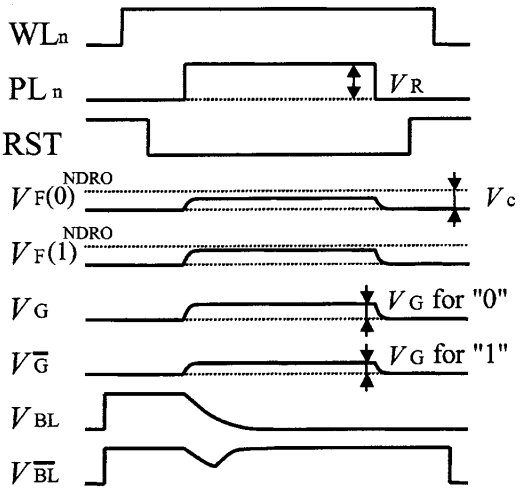

Figure 7. Pulse sequence for the NDRO operation.

Next, V_R^{MIN} for each bit was measured. Finally, the highest V_R^{MIN} was chosen. Figure 8 shows the behavior of the highest V_R^{MIN} in 64 K bits of FeRAM using symmetrical and asymmetrical program scheme as functions of storage time. The highest V_R^{MIN} increases with storage time gradually, when the NDRO FeRAM uses symmetrical program scheme, because hysteresis loop has been deformed by the imprint effect toward the positive voltage direction. On the other hand, the highest V_R^{MIN} of the NDRO FeRAM using asymmetrical program scheme decreases gradually with storage time, because the hyteresis loop

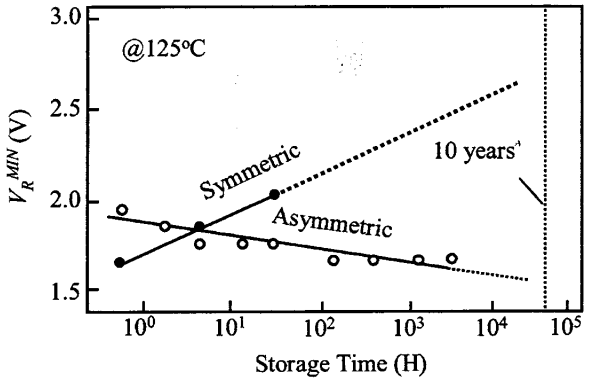

Figure 8. Time dependence on readout minimum voltage of a worst bit. In symmetric programming, the V_R^{MIN} increases with storage time. In asymmetric programming, the V_R^{MIN} decreases with storage time.

has been deformed by the imprint effect toward the negative voltage direction only.

When the NDRO FeRAM uses the asymmetrical program scheme, the value of V_R, is lowered by the imprint effect from 2.8 V to 2.0 V. As a result, using the asymmetrical program scheme, the power consumption on reading can be reduced for approximately 35 percents. Consequently, NDRO with asymmetrical program scheme meets the requirements from low power applications such as mobile devices. Further, because the readout signal can be increased by using the scheme, some originally small readout signals can be also increased. Therefore, when we employ this asymmetrical program scheme intentionally before shipment, the production yield rate can be raised.

V. CONCLUSIONS

In this paper, we described that nondestructive readout using asymmetrical program scheme was developed to minimize the imprint effect. Using asymmetrical program scheme, operation voltage will be lowered from 2.8 V to 1.8 V. Thereby, the power consumption on reading in FeRAM can be reduced for approximately 35 percents. As a conclusion, we can improve the imprint endurance in a NDRO FeRAM using asymmetric program scheme. Also, we showed that asymmetrical program scheme is one of solutions to attain the low powered portable terminals.

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