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LETTER

Fast Pulse Driving of Ferroelectric SBT Capacitors in a Nonvolatile Latch

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SUMMARY We demonstrate a fast shutdown and resumption of a logic circuit applied a nonvolatile latch having $SrBi_2(Ta,Nb)_2O_9$ (SBT) capacitors without a higher drive voltage than a logic voltage of 1.8 V. By assigning an individual drive circuit of the SBT capacitors to the nonvolatile latch not sharing a drive circuit with multiple nonvolatile latches, the fast shutdown and resumption of a logic circuit were completed in 7.5 ns at a drive voltage of 1.3 V. The fast shutdown and resumption without an addition of a high drive voltage to a logic circuit meets a requirement from power-saving applications of system LSIs fabricated in CMOS technologies at 90-nm and below.

key words: *nonvolatile latch, SBT, fast resumption, power management*

1. Introduction

To reduce power consumption of system LSIs, power management for a logic circuit has been mainly focused on reducing dynamic power consumption during data processing [1]. Along with scaling of the CMOS technology, an increase of the power consumption of a logic circuit during data processing is suppressed because a logic voltage becomes lower. Contrary to this, idle power consumption has increased for a leakage current along with the scaling of the CMOS technology from 90-nm and beyond. Consequently, the issue of the idle power consumption due to the leakage current becomes serious concerns [2], [3].

Multi-threshold CMOS (MTCMOS) technology provides a low leakage current of a logic circuit and high performance operation by utilizing high speed, low threshold voltage (V_t) transistors for a logic circuit and high V_t transistors for a power switch [4]. During an idle state, a power switch disconnects a logic circuit from a power supply and/or ground to reduce the leakage current. In an active state, by turning on the power switch, a low V_t transistors in a logic circuit realizes high speed operation. However, by using the MTCMOS technology, data at a sequential circuit can not be retained without power supply during the idle state.

To retain data at a sequential logic circuit even in the idle state, variable threshold CMOS (VTCMOS) technology has been reported [5], [6]. In the technology, varying V_t in a logic circuit dynamically by applying multiple back gate biases, low leakage current is consistent with high speed operation in a same logic circuit. During data processing, the subthreshold voltage is lowered so that a circuit operates fast. On the other hand, in an idle state, to minimize the subthreshold currents, a proper voltage is applied to a body so that the subthreshold voltage becomes larger. However, along with a development of the CMOS technology, a low supply voltage of about 1 V, and a short channel effect increases a difficulty of predicting precise V_t [7]. Further, the dynamic power management using the VTCMOS technique can not eliminate completely the tunneling currents through thin gate dielectrics during an idle mode, which increases idle power consumption. Consequently, the idle power consumption due to the tunneling current increases seriously. The increase of the idle power consumption does not meet a requirement from high performance low power applications.

To eliminate the subthreshold current and the tunneling current, a nonvolatile latch having ferroelectric capacitors has been proposed [8]–[10]. By using the nonvolatile latch, we can completely shut off a power consumption of a logic circuit by storing data to ferroelectric capacitors. The nonvolatile latch is composed of a latch holding a logic status during a period in existence of a supply voltage and ferroelectric capacitors holding the logic status in the absence of a supply voltage. Prior to the idle state, a logic status held at a latch is transferred to the ferroelectric capacitors. Then, the supply voltage can be removed completely during the idle state. Therefore, we can eliminate the idle power consumption by applying the nonvolatile latch into a logic circuit.

However, as long as we apply conventional nonvolatile latch having Lead Zirconate Titanium ($PbZrTiO_3$: PZT) capacitors into a logic circuit, the PZT capacitors can be driven at a high voltage of 3.3 V but can not be driven at a logic voltage of 1.8 V [8]. Therefore, to transfer a logic status into the PZT capacitors, we need different voltages in the circuit system which uses nonvolatile latch with PZT capacitors.

The switching time for polarization reversal in ferroelectric films of PZT is smaller than 1.8 ns [11]. However, a conventional transition time of a logic status using an NVLT with PZT capacitors shows 100 ns [9], which is slow compared with a system clock used in system LSIs fabricated at 90-nm CMOS technology and beyond [12].

Therefore, to integrate the nonvolatile latch into system LSIs whose system clock is faster than the 100 ns, we need to investigate the smaller limit of transition time aiming for several nanoseconds almost equal to a switching time of a polarization reversal.

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In this paper, we developed a nonvolatile latch having 100-nm thickness Strontium Bismuth Tantalate ($SrBi_2(Ta,Nb)_2O_9$: SBT) capacitors prepared by spin-on and metal-organic deposition. The nonvolatile latch can operate in a 1.8 V logic voltage of 0.18-μm CMOS technology. Moreover, to transfer a logic status from SBT capacitors to a latch or from a latch to SBT capacitors as fast as a system clock in system LSIs, we connected a drive circuit to SBT capacitors directly. Consequently, by driving SBT capacitors in a nonvolatile latch, the transition of a logic status is completed within 7.5 ns.

2. Power Management Using Nonvolatile Latch

Figure 1(a) shows a circuit schematic of a logic circuit applied nonvolatile latches (NVLTs), which is composed of sequential logic circuits and combinational logic circuits, a power switch and a power controller. The power controller can judge whether the power switch should be turned on or off by detecting a logic input status. In addition, latches have the nonvolatile memory in their own cell area to hold a logic status without a supply voltage during an idle state.

During data processing, the power controller turns the power switch on, and NVLTs hold a logic status by using a supplied power as normal latches do. When a logic block goes into an idle state, a logic status at the latches is transferred to a nonvolatile memory attached in each NVLT. After the moment, by turning the power switch off, the power of the logic block is completely shut off to eliminate a leakage current during the idle state. Here, a power consumption of the logic block in the idle state is cut down completely. Then, when input signals enter the logic block again, operation state goes from the idle state to data processing. At that, a logic status held in the nonvolatile memory is recalled into a latch of NVLTs, then, data processing is restarted.

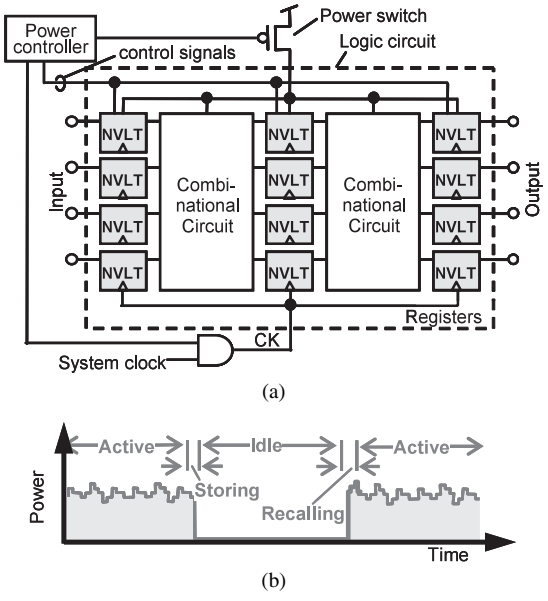

Fig. 1 (a) Logic circuit using nonvolatile latches. (b) Power reduction during shutdown.

Figure 1(b) shows an image of power reduction, when we operate shutdown and resumption of logic circuits in Fig. 1(a). During data processing, power consumption of a logic circuit applied NVLTs is as much as that of a logic circuit applied normal latch. When input signal are not entered into the circuit, the circuit is in the idle state. At the time, the power-switch is turned off to stop supplying the power to the circuit, and the power consumption of the circuit becomes zero completely. When the NVLT is not applied into the circuit, the static power consumption by a subthreshold current and a tunneling current is caused in the idle state. The power consumption will increase in system LSIs fabricated in 90-nm CMOS technology and beyond. After the idle state, when the input signal is entered into the logic circuit, the logic circuit recalls the logic status stored in the NVLT. Then, the logic circuit restarts operation, and the dynamic power consumption is caused in the logic circuit. In this manner, a logical circuit applied NVLTs repeats the data processing and the idle state to eliminate power consumption during the idle state. Therefore, in the case of logic circuits fabricated in 90-nm CMOS technology and beyond where tunneling currents through thin gate dielectrics become large, it is important to reduce the power consumption of the circuit in the idle state.

Here, when NVLTs are applied into a logic circuit, power consumption during the store operation and the recall operation may increase due to a drive operation of ferroelectric capacitors in a latch. However, by a circuit design using a block-by-block power controller for preventing an increase of power consumption in a logic circuit, power management can suppress a peak power of the logic circuit.

3. Conventional Issues in a Nonvolatile Latch

When the NVLT having ferroelectric capacitors is applied into a logic circuit, it is advantageous for a cost of chip area to drive ferroelectric capacitors without a high voltage. Conventionally, a nonvolatile latch fabricated in a 0.18-μm FeRAM technology using lead zirconate titanate (PZT) capacitors has been proposed [6]. However, the coercive voltage of the PZT capacitor, which is a minimum voltage to bring a fully switched polarization to zero, is a voltage of about 1.1 V. Accordingly, to reverse the polarization, the PZT capacitor needs a high voltage of 3.3 V, which is higher than a logic voltage of 1.8 V. The necessity of two different voltage leads to complexity of a circuit design using two types of drive circuit of a logic voltage and of a drive voltage to ferroelectric capacitors. This requires additional process technologies for a low voltage circuit and a high voltage circuit.

Next, we explain an issue of operation speed of a conventional NVLT. System LSIs fabricated in CMOS technologies at 90-nm and beyond operate in several hundreds MHz. Let's suppose that the NVLTs are applied into the logic circuits of the system LSIs for applications of dynamic power management in which shutdown and resump-

tion are repeated frequently [1]. When input signals are entered synchronized with a several hundreds MHz frequency and a transition time of a logic status is longer than a cycle time of the hardware frequency, a transition time of recalling the logic status and a system clock time of input signals are unmatched. Therefore, because the unmatched timing is needed to be adjusted, a coprocessor is needed to control input signals on recalling. In contrast, if a transition time of a logic status is equal to a cycle time of a several hundreds MHz frequency, we can attain that the transition time of a logic status equally to a system clock time of a hardware using the gated clock. So, the coprocessor for the power management becomes unnecessary. However, a conventional NVLT demonstrated up to 100 ns as a store time and a recall time. Therefore, we need to investigate whether NVLTs in a logic application can keep up with the system clock in a system LSI fabricated with 90-nm CMOS technology and beyond.

4. Approach to Low Voltage Operation

Figure 2 shows a circuit schematic of the nonvolatile latch. We embedded a driver circuit into an NVLT cell to drive ferroelectric capacitors fast. Also, SS switches disconnect ferroelectric capacitors to prevent form a fatigue on ferroelectric capacitors during an active mode.

A typical pulse sequence of the NVLT for power saving is shown as Fig. 3. During an active state, by turning off SS switches, the NVLT can operate as a normal latch which can hold a logic status synchronizing an input clock signal. Prior to the idle state, logic data at nodes N and XN are stored into the ferroelectric capacitors by turning on SS switches and applying voltage pulses to PL1 and PL2. Then, the device power is removed. By doing so, a polarization is stored as a logic status to ferroelectric capacitors. In Fig. 2, arrows mean the direction of the polarization after storing when the node N is high and the node XN is low. To return the logic status as before, the stored data are recalled from the ferroelectric capacitors to nodes N and XN by applying a voltage pulse to PL1 keeping PL2 grounded. The voltage pulse converts the polarization of the ferroelectric capacitors into a differential readout voltage between nodes N and XN.

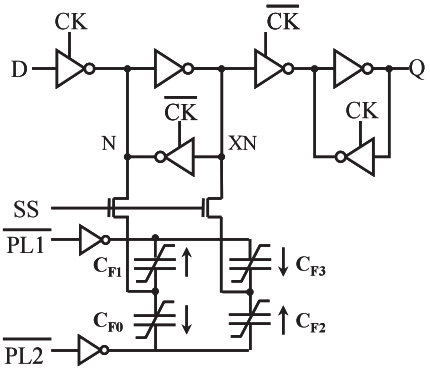

Fig. 2 A circuit schematic of a nonvolatile latch.

Then, when a power is supplied to the NVLT, cross-coupled inverters in the NVLT can be operated as a sense amplifier. Therefore, the differential readout voltage is amplified to a supply voltage or is grounded as before.

Next, to lower a drive voltage for transition of a logic status to the logic voltage used in the system LSI, we investigate a relationship between a differential readout voltage of an NVLT and a ferroelectric property. A motion of operation points in the circuit are shown in Fig. 4. An upper-right, upper-left, lower-right, and lower-left hysteresis loop correspond to C_{F1}, C_{F2}, C_{F3}, and C_{F4} respectively. Solid lines show motions of operation points when a drive voltage (V_{DR}) is applied to an NVLT. Dotted lines show approximated linear lines of operation points. From this figure, because solid lines are almost equal to dotted lines, we can simplify the motion of operation points as linear lines. When the amount of charge can be placed on a series con-

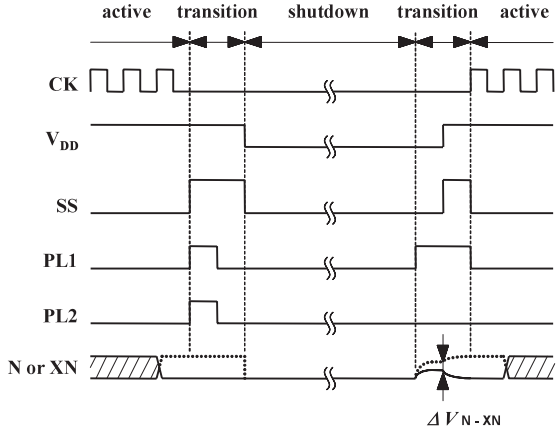

Fig. 3 Pulse sequence of a nonvolatile latch.

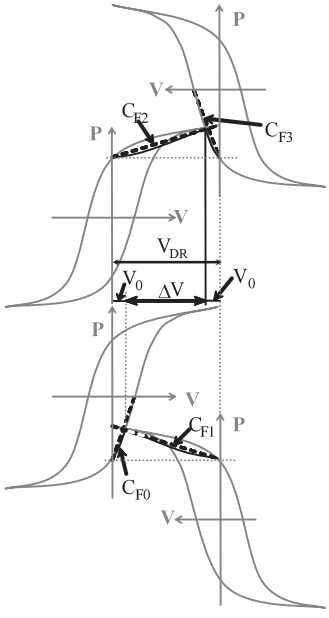

Fig. 4 Motion of operation points in a nonvolatile latch and differential voltage between nodes N and XN.

nection of C_{F0} and C_{F1} on reading, the following equation is given by

$$C_{F0} \cdot V_0 = C_{F1} \cdot (V_{DR} - V_0), \quad (1)$$

where C_{F0} and C_{F1} are the capacitance in Fig. 2, which are correspondent with the direction of a stored polarization. V_0 is the voltage of a center node of a series connection of C_{F0} and C_{F1}. V_{DR} is a drive voltage between PL1 and PL2. Then, because C_{F0} and C_{F1} equals C_{F3} and C_{F2} respectively, the differential voltage between a node N and a node XN, ΔV, before amplified by cross-coupled inverters in an NVLT is derived as following Eq. (2).

$$\Delta V = V_{DR} - 2 \cdot V_0. \quad (2)$$

Next, using Eq. (1), the readout differential voltage ΔV is given by

$$\Delta V = \frac{C_{F0} - C_{F1}}{C_{F0} + C_{F1}} \cdot V_{DR}. \quad (3)$$

Here, C_{F0} and C_{F1} are approximated a linear paraelectric capacitance and a linear ferroelectric capacitor as shown in dotted lines in Fig. 4 respectively, because readout motion of an operation point of C_{F0} is preferably small and C_{F1} is not reversed. So, the following Eq. (4) is given by

$$\Delta V = \frac{\frac{P_r \cdot S}{V_c} - \frac{\varepsilon \cdot S}{t}}{\frac{P_r \cdot S}{V_c} + \frac{\varepsilon \cdot S}{t}} \cdot V_{DR}, \quad (4)$$

where P_r is remnant polarization, V_c is a coercive electric voltage of ferroelectric capacitors, ε is a permittivity of a linear capacitance of ferroelectric capacitors, S is a area of a ferroelectric capacitor and t is a thickness of a ferroelectric capacitor. Finally, Eq. (4) is adjusted, the following equation is derived.

$$\Delta V = \frac{\frac{P_r}{E_c} - \varepsilon}{\frac{P_r}{E_c} + \varepsilon} \cdot V_{DR} = \frac{\frac{P_r}{E_c} - \varepsilon_0 \cdot \varepsilon_r}{\frac{P_r}{E_c} + \varepsilon_0 \cdot \varepsilon_r} \cdot V_{DR} = \alpha \cdot V_{DR}, \quad (5)$$

where E_c is a coercive electric field of ferroelectric capacitors at the thickness of ferroelectric capacitor t, ε_0 is a vacuum permittivity, ε_r is a ferroelectric relative permittivity and α is a coefficient of a readout differential voltage which is determined by properties of ferroelectric materials. From Eq. (5), ΔV depends on P_r, E_c and ε_r at the same film thickness. For instance, we compare ΔV of typical ferroelectric materials, PZT and SBT. Generally, when P_r is high, E_c tends to be higher than that in case of low P_r [13], [14]. Table 1 shows general properties of 100-nm thickness PZT capacitors and 100-nm thickness SBT capacitors fabricated using MOD (metal-organic deposition) process. From this table, P_r of PZT is larger than that of SBT. On the other hand, E_c of SBT is smaller than that of PZT. Equation (5) and Table 1 shows that not only P_r, but also E_c and ε_r decide α, namely ΔV in the NVLTs. Figure 5 shows the result

Table 1 Properties of general ferroelectric materials and coefficient of differential readout voltage of an NVLT using 100-nm thickness SBT capacitors and 100-nm thickness PZT capacitors. Both capacitors were fabricated using MOD process.

	SBT(MOD)	PZT(MOD)
P_r (μC / cm^2)	7	14
E_C (kV / cm)	60	105
ε_r	300	430
α	0.63	0.50

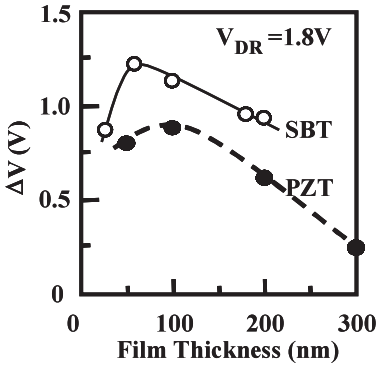

Fig. 5 Thickness dependence of ΔV for SBT and PZT.

of a calculated differential readout voltage using Eq. (5) in case that PZT capacitors or SBT capacitors are applied to the NVLT. When we estimate the differential readout voltages in the nonvolatile latch at the same film thickness of ferroelectric capacitors, the differential readout voltage using SBT capacitors becomes about 300 mV higher than that of PZT capacitors at the same thickness of ferroelectric capacitors. From this result, an NVLT using SBT capacitors suits for low voltage operation compared with an NVLT using PZT capacitors. Consequently, to equate a drive voltage in a logic circuit and a voltage to drive ferroelectric capacitors.

5. Fast Transition of Logic Status

In the field of a nonvolatile memory such as FeRAM, data retention time is required for longer than 10 years. Therefore, an applied pulse width to ferroelectric capacitors is needed for longer than 100 ns [15]. On the other hand, in the field of dynamic power management, because the purpose of the power management is temporal data storage, data retention time is required for a few minutes at most. Rather than extending the data retention time, the fast transition of a logic status is required [5]. Therefore, we aimed at developing a fast transition of a logic status by connecting directly the drive circuit with an individual ferroelectric capacitor, and minimizing parasitic resistance and capacitance. In order to investigate the improved fast transition time, using 0.18-μm FeRAM technology [16], we designed and fabricated NVLTs where drive circuits are directly con-

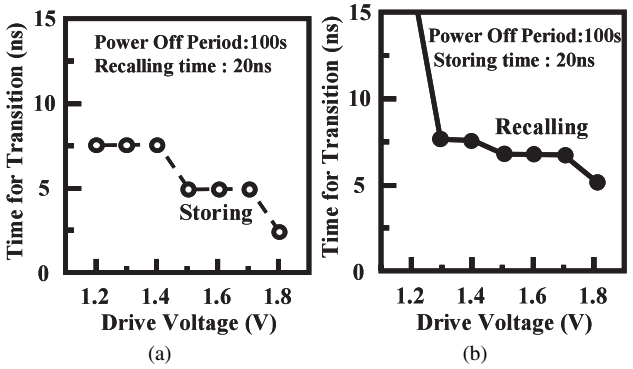

Fig. 6 Transition time vs. drive voltage for (a) storing and (b) recalling.

nected to SBT ferroelectric capacitors in the NVLTs. Area of an SBT capacitor is 1.2 μm^2 and SBT film thickness is 100 nm. An SBT film of ferroelectric capacitors is prepared by spin-on and metal-organic deposition.

Providing 100 seconds for the shutdown period, we store the logic status and restore the logic status. Figures 6(a) and (b) shows the minimum store time as a function of a drive voltage and the minimum recall time as a function of a drive voltage respectively. At the drive voltage of a standard logic voltage of 1.8 V at 0.18-μm CMOS technology, a store time and a recall time can be realized 2.5 ns and 5.0 ns respectively. Compared with a transition time of conventional ferroelectric RAM application, 100 ns, using a drive voltage of 3.3 V to PZT capacitors, the fast transition time under 10 ns is about 10 times faster. The first reason why such a fast transition can be achieved is that drive circuits are directly connected to ferroelectric capacitors in the each NVLT. In addition that, we can presume that polarization switching speed of SBT takes only several nanoseconds during the store and recall transition. Furthermore, the drive voltage of 1.3 V is lower than that of a conventional nonvolatile latch using PZT capacitors. This is because the coercive voltage of SBT capacitors is lower than that of PZT capacitors. From this result, we confirmed that a drive voltage of ferroelectric capacitors, 1.3 V, equals with a supply voltage of the logical circuit fabricated at 0.13-μm CMOS technology. In addition, the logic status can be transferred in 10 ns or less. An NVLT applied SBT capacitors well meets a speed of sytem LSIs clocked at a several hundreds MHz.

6. Conclusion

The fast shutdown and resumption of a logic circuit using nonvolatile latches having 100-nm thickness SBT capacitors is completed within 7.5 ns in a low voltage operation such as 1.3 V. We can presume that by applying a thinner SBT film, further low voltage operation of a nonvolatile latch can be realized. Therefore, by applying the nonvolatile latch using SBT to system LSIs fabricated in 90-nm CMOS technology and beyond, we can contribute reduction of the idle power consumption during an idle state.

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