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Nonvolatile Memory Using Epitaxially Grown Composite-Oxide-Film Technology

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We have developed a ferroelectric-gate field-effect transistor (FeFET) composed of heteroepitaxially stacked oxide materials. A semiconductor film of ZnO, a ferroelectric film of Pb(Zr,Ti)O_3 (PZT), and a bottom gate electrode of $SrRuO_3$ (SRO) are grown on a $SrTiO_3$ (STO) substrate. Structural characterization shows a heteroepitaxy of the fabricated ZnO/PZT/SRO/STO structure with good crystalline quality and the absence of an interface reaction layer. When the polarization direction of the PZT film is downward, all the electrons across the ZnO film are depleted. When the polarization direction is upward, on the other hand, quasi-two-dimensional electron gas is accumulated at the ZnO/PZT interface. The switching of the quasi-two-dimensional electron gas between the two states is confirmed by capacitance–voltage measurements. Drain and source electrodes of Pt/Ti are formed on the ZnO film and in-plane conduction at the ZnO/PZT interface is probed. When gate voltages applied to the bottom electrode are swept between −10 and 10 V, the on/off ratio of drain currents is higher than 10^5. Such a high on/off ratio is preserved even after 10^5 s and the extrapolation of the retention behavior predicts a definite memory window of more than 10 years. [DOI: 10.1143/JJAP.47.2719]

KEYWORDS: ferroelectric, ferroelectric-gate field-effect transistor, two-dimensional electron gas, interface conduction, ZnO, $SrTiO_3$, $SrRuO_3$, Pb(Zr,Ti)O_3, epitaxial growth, nonpolar

1. Introduction

The two-dimensional electron gas that accumulates at the interface between two insulating oxides is drawing considerable attention because of its attractive applications in electric devices.[1,2] The conductivity of the electron gas can be modulated from an insulating state to a metallic state by applying an electric field on a gate electrode.[3] Such phenomena can be developed to produce a new type of a nonvolatile memory by replacing one of the stacked dielectric oxides with a ferroelectric oxide. We can switch the conduction states by polarization reversal, and the binary states are preserved by the remnant polarization of the ferroelectric oxide even when gate voltage is removed.

Such an in-plane electrical transport property on the surface of a ferroelectric single crystal under ultrahigh vacuum has already been reported by Watanabe *et al.*[4] Surface conduction was well controlled by polarization direction. When the ferroelectric crystal was homogeneously polarized, a conductive state was preserved for 12 days. For a randomly polarized crystal, on the contrary, conductivity rapidly decreased. On the basis of the in-plane conduction switching on the ferroelectric, a variety of types of ferroelectric-gate field-effect transistors (FeFETs) composed of different stacked structures have been investigated.[5–7] For example, a FeFET with an insulator/ferroelectric structure having drain and source electrodes at the interface has been formed on a bottom gate electrode of Pt.[6] The drain currents of this FeFET show hysteresis loops and a maximum on-current/off-current (I_{on}/I_{off}) ratio of higher than 10^5 is obtained by applying a certain gate voltage. However, the difference in the drain currents between the binary states at a zero gate voltage, which is indispensable for nonvolatile memories, is not sufficiently large owing to a shift in the threshold voltage. Such a shift in the threshold voltage suggests the existence of space charge in the ferroelectric film or at the insulator/ferroelectric interface. Since the drain and source electrodes were formed on the ferroelectric before the deposition of the upper insulator film, we speculate that the generation of the space charge can be attributed to surface damage of the ferroelectric incurred by the formation of the electrodes. Thus, we consider that the continuous growth of a stacked structure is needed to form a clean interface. Up to now, a retention property of this type of FeFET has not been reported. Tokumitsu *et al.* reported another type of FeFET with a stacked semiconductor/ferroelectric structure having top drain/source electrodes and a bottom gate electrode.[7] The in-plane conduction current on the ferroelectric was probed using the top drain/source electrode, and a definite I_{on}/I_{off} ratio of the drain currents was obtained at a zero gate voltage. Since no shift in the threshold voltage appeared in the FeFET, the directly stacked semiconductor/ferroelectric structure is considered to be effective for forming a clean interface. However, the retention property of the FeFET was insufficient to put it to practical use. We consider that the poor retention property of the FeFET fabricated on a bottom gate electrode can be attributed to the coarse interface and random orientation of the ferroelectric from the results of Watanabe's work,[4] since ferroelectric films formed on metals have polycrystalline structures in general.[8] Flat interfaces can be attained for top-gate-type FeFETs fabricated on silicon substrates, which have metal/ferroelectric/semiconductor (MFS) structures.[9] However, the realization of MFS-based FeFETs faces difficulties in terms of controlling the ferroelectric/semiconductor interface, which is vital for attaining good retention characteristics.[9,10] Growing the ferroelectric gate directly on the silicon substrate resulted in unstable channel characteristics owing to the existence of interface oxide layers. Although channel stabilization can be achieved by inserting a buffer layer between the ferroelectric and the silicon substrate,[11–14] a built-in potential across such a stack structure gives rise to a depolarization field and leakage currents, which are detrimental to the retention properties.

On the basis of the previous studies, we can summarize four requirements for developing a FeFET with a good retention property, namely, a directly stacked structure, homogeneous polarization, a flat interface, and no interface reaction layer. In this work, we have challenged a perfect solution for these vital requirements. For the first require-

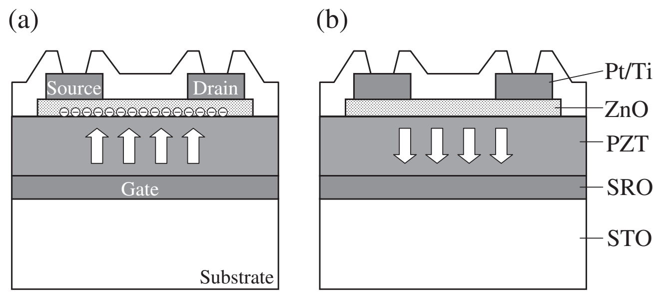

Fig. 1. Schematics of (a) on state (two-dimensional electron accumulation) and (b) off state (electron depletion) of FeFET.

ment of the directly stacked structure, we chose an n-type oxide semiconductor, ZnO, film stacked on a ferroelectric $Pb(Zr_{0.52},Ti_{0.48})O_3$ (PZT) film. In order to probe the in-plane conduction at the interface of the stacked structure, drain and source electrodes of Pt/Ti, of which the adhesion layer of Ti is a low-work-function material,[15] were formed on the ZnO surface. For the second requirement, the homogeneous polarization of the PZT, and the third requirement, the flat interface, we chose $SrRuO_3$ (SRO) as a bottom gate electrode and $SrTiO_3$ (STO) as a substrate, respectively, which are perovskite materials, similar to PZT. Therefore, we can expect the heteroepitaxial growth of the PZT/SRO/STO structure with a homogeneous crystal orientation, i.e., homogeneous polarization, and a flat surface. For the fourth requirement, no interface reaction layer, the ZnO film was continuously grown on the stacked perovskite structure *in situ* at a growth temperature lower than that used for depositing the underlying films. As a result, we have achieved a heteroepitaxy of a nonpolar-ZnO/PZT/SRO/STO structure. The interface is atomically flat and no undesirable interface layer is observed between the ZnO film and the PZT film. The switching of the quasi-two-dimensional electron gas between accumulation and depletion states (Fig. 1) is successfully confirmed by capacitance–voltage (C–V) measurements. A fabricated FeFET with a 30-nm-thick ZnO film, whose carrier density is as low as $\sim 10^{15}\,\mathrm{cm}^{-3}$, exhibits a high I_{on}/I_{off} ratio of more than 10^5 and shows no shift in its threshold voltage. Furthermore, a long retention time, longer than 10^5 s, with an I_{on}/I_{off} ratio of 10^4 was achieved. Such good retention properties can be attributed to the strong coupling between the polarization of the PZT film and the accumulated electron layer.

2. Experimental Procedure

The transistors were fabricated on $15 \times 15\,\mathrm{mm}^2$ Nb-doped STO(001) single-crystal substrates that were polished and etched by the vendor (Shinkosha) and showed atomically flat surfaces. The STO substrates were mounted in a vacuum chamber initially evacuated to a pressure on the order of 10^{-6} Torr. Stacked films of a 30-nm-thick SRO film (gate electrode), a 450-nm-thick PZT film, and a 30-nm-thick ZnO film were deposited *in situ* on the STO substrates by pulsed laser deposition (PLD) utilizing a KrF excimer laser source ($\lambda = 248$ nm, LPX210). During the SRO deposition, the oxygen pressure was 10 mTorr and the substrate temperature was held at 700 °C. The energy density on the surface of the ceramic ablation target was $\sim 1.0\,\mathrm{J/cm}^2$ and the repetition rate was 5 Hz. PZT deposition was conducted at the same temperature (700 °C) and an oxygen pressure of 100 mTorr. The energy density was $\sim 1.0\,\mathrm{J/cm}^2$ and the repetition rate was 10 Hz. Afterward, the substrate temperature was changed to 400 °C. The ZnO film was deposited on the PZT/SRO/STO structure at an oxygen pressure of 10 mTorr. The energy density was $\sim 0.5\,\mathrm{J/cm}^2$ and the repetition rate was 10 Hz. Then a photoresist mask was formed on the surface by standard photolithography followed by the wet etching of the ZnO film with diluted nitric acid. Finally, Pt/Ti source and drain contacts were formed on the ZnO film by electron-beam evaporation and a silicon nitride layer was deposited by rf sputtering for passivation. The fabricated transistor had a channel length of 3 µm and a width of 100 µm. For the electrical characterization of the PZT film, a Pt/Ti/PZT/SRO/STO structure was also fabricated by depositing a top Pt/Ti electrode on the ZnO-etched surface.

Structural characterization of the films was carried out by X-ray diffraction (XRD) analysis and by cross-sectional transmission electron microscopy (TEM). Transmission electron diffraction (TED) analysis was also performed to evaluate the epitaxial structures of the films. The surface morphology and orientation were investigated by atomic force microscopy (AFM) and electron beam backscattering pattern (EBSP) analysis, respectively.

The carrier concentration, mobility, and resistivity of the ZnO films were determined by the van der Pauw method at room temperature using Hall-effect measurement equipment (Accent HL5500PC). In order to study the thickness dependence of the electric characteristics of ZnO, ZnO films with different thicknesses were prepared for these measurements by controlling the deposition time. Polarization–voltage (P–V) characteristics of the Pt/Ti/ZnO/PZT/SRO/STO structure and the Pt/Ti/PZT/SRO/STO structure were measured by applying 1-kHz rectangular ac voltage pulses with a ferroelectric test system (Radiant RT6000SI). C–V measurements were also conducted by applying a small alternating signal of 30 mV using an LCR meter (Agilent 4284A). Drain current–voltage (I_{ds}–V_{gs}) characteristics were measured using a semiconductor parametric analyzer (Agilent 4155C).

3. Results and Discussion

3.1 Structural characterization

Large-angle X-ray scans (10 to 80°) shows only (00l) pseudo-cubic reflections from the stacked perovskite structure, namely, PZT/SRO/STO, and a (11$\bar{2}$0) reflection from the wurtzite ZnO film (Fig. 2). The full width at half-maximum (FWHM) values of the PZT(003) and ZnO(11$\bar{2}$0) peaks are as low as 37 and 72 arcsec, respectively. We observed no reflections indicating second phases. Thus, the SRO, PZT, and ZnO films are preferentially grown along (001), (001), and (11$\bar{2}$0) directions, respectively. A cross-sectional dark-field TEM image and cross-sectional bright-field TEM images of the heterostructure are shown in Fig. 3(a) and Figs. 3(b) and 3(c), respectively. The high-resolution image in Fig. 3(b) reveals that no undesirable layer at the ZnO/PZT interface was present and the ZnO film apparently keeps the periodic lattice structure on the PZT film. Therefore, excellent physical and electrical properties for the interface are expected.

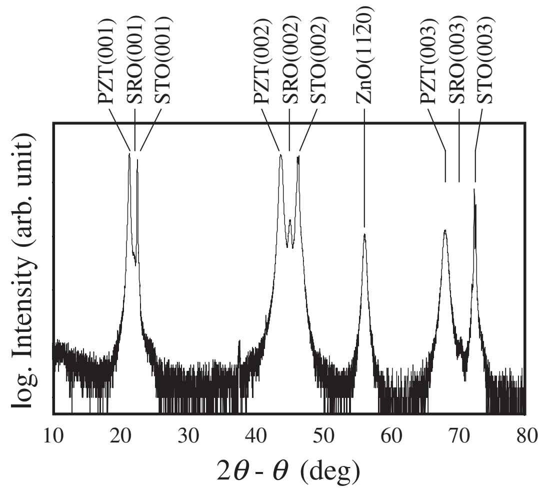

Fig. 2. XRD spectra from ZnO/PZT/SRO/STO structure.

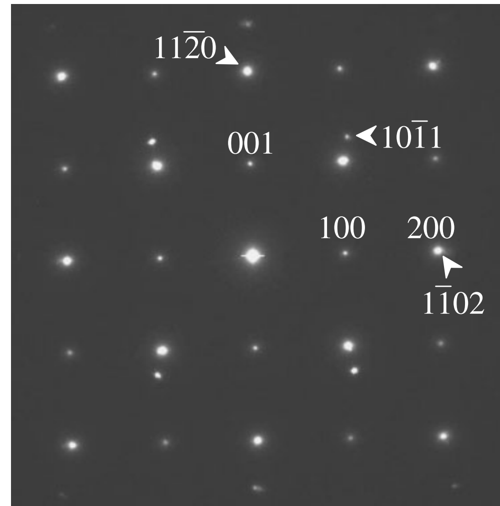

Fig. 4. TED spots related to plane indices of ZnO (arrows) and PZT.

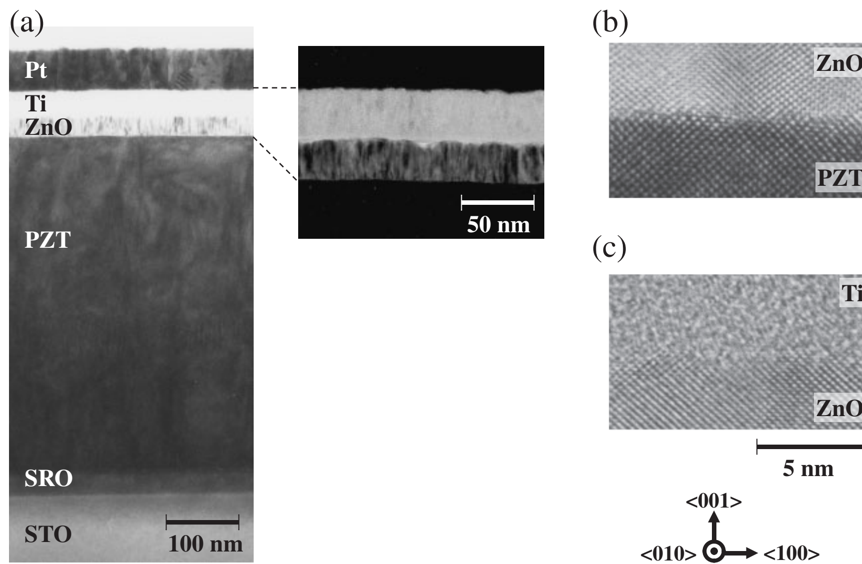

Fig. 3. Cross-sectional TEM images of (a) Pt/Ti/ZnO/PZT/SRO/STO structure and higher magnifications of (b) ZnO/PZT and (c) Ti/ZnO interfaces.

Selected-area electron diffraction patterns of the PZT and ZnO films were obtained from a (010) cross section of the STO substrate by TED analysis. Since only diffraction spots appear in the diffraction image of Fig. 4, we can confirm the single-crystalline quality of the PZT and ZnO films. The TED patterns also indicate that ZnO[1$\bar{1}$02] is parallel to PZT[100]. From these experimental results and previously reported lattice parameters,[16,17] lattice matching between the PZT and ZnO films can be assumed to be as illustrated in the diagram in Fig. 5. Although the mismatch is as large as 5.1%, we observed no grains with different orientations by a pole figure measurement of EBSP (scanned area is $5 \times 5\,\mu m^2$). In addition, the measured rms value of the surface roughness is as small as 0.815 nm, which indicates that the heterostructure has a nearly atomically flat surface. Although the PZT film was deposited beyond the critical thickness, which was calculated to be ~6 nm on the basis of the Matthews–Blakeslee model,[18] we conclude that the stacked ZnO/PZT/SRO structure is heteroepitaxially grown on the STO substrate. We considered that such heteroepitaxy can be attributed to nonequilibrium growth during the deposition.[19]

It should be emphasized that the *c*-axis of the ZnO film, along which a spontaneous polarization of $5.7\,\mu C/cm^2$ appears,[20] is perpendicular to the polarization axis (*c*-axis) of the PZT film. So far, the *c*-axis orientation of ZnO has been studied for providing ultraviolet light-emitting devices and high-speed switching devices.[21–24] For instance, Tsukazaki *et al.* reported the quantum Hall effect in polar $ZnO/Mg_xZn_{1-x}O$ heterostructures, in which confined electrons in a two-dimensional layer at the interface can move within the layer with minimal scattering.[24] In contrast, we intend to accumulate a two-dimensional electron gas at the ZnO/PZT interface using the polarization switching of PZT. To prevent the interaction of the spontaneous polarization of ZnO with the polarization switching of PZT, such a system requires a nonpolar ZnO film. In this work, we have successfully realized nonpolar-ZnO/PZT heteroepitaxy with

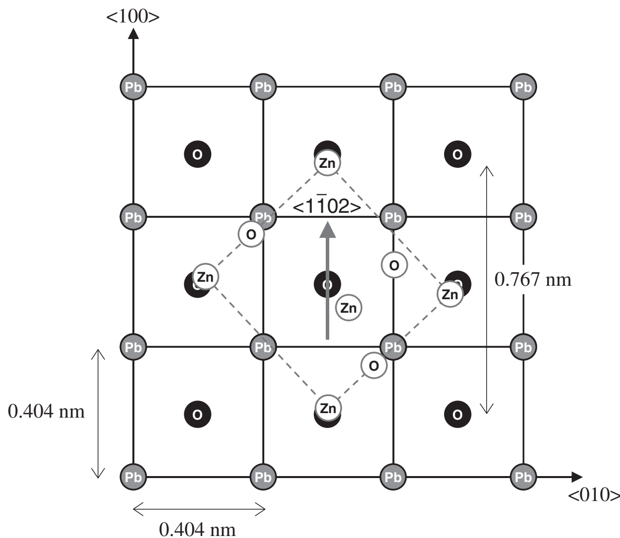

Fig. 5. Schematic representation of lattice matching between ZnO and PZT.

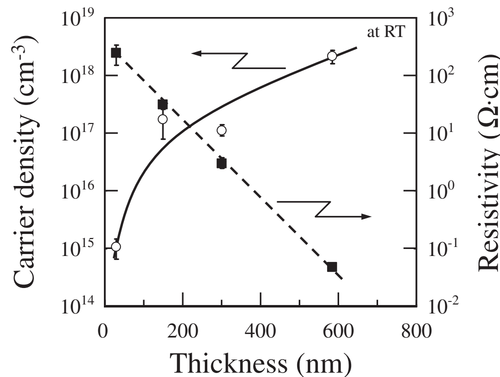

Fig. 6. Carrier density and resistivity of ZnO films as function of film thickness.

good crystallinity. Thus, we can expect good electrical property and retention characteristics for FeFETs composed of the nonpolar-ZnO/PZT/SRO structure.

3.2 Electrical characterization

Because the first deposited layer of SRO has a role of a gate electrode, which requires a low resistivity for fast driving, we measured the resistivity of the 30-nm-thick SRO film. The measured resistivity was $6.6 \times 10^{-6}\,\Omega\,\text{m}$, which is as low as that of a bulk SRO, i.e., $2.8 \times 10^{-6}\,\Omega\,\text{m}$.[25]

For the electrical characterization of the channel layer in the FeFET, the carrier density and resistivity of ZnO films with different thicknesses were measured using the van der Pauw method at room temperature (Fig. 6). The resistivity of the ZnO film increases with a decrease in the film thickness, while the carrier density decreases. The carrier density at 30 nm is as low as about $10^{15}\,\text{cm}^{-3}$, which is much lower than those in previous reports.[20,26] We speculate that such a low carrier density is due to the epitaxial growth of the ZnO film with a good crystalline quality. Because the current magnitude at an off state depends on the resistivity of the ZnO channel, we chose a 30-nm-thick ZnO film, which

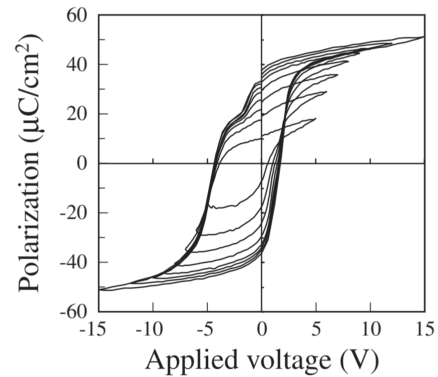

Fig. 7. *P–V* hysterisis curves of Pt/Ti/ZnO/PZT/SRO capacitor.

exhibits the highest resistivity in our experiments, to incorporate in a FeFET. The electron mobility along the *c*-axis of the 30-nm-thick ZnO film was measured and found to be $26\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$, which is almost equivalent to the previously reported values along the *a*-axis of ZnO films thicker than that used in this work.[27]

Ferroelectric hysteresis (*P–V*) measurements were carried out on a Pt/Ti/ZnO/PZT/SRO capacitor by applying voltages to the SRO electrode with the Pt/Ti electrode grounded. The film thickness of the ZnO film is 30 nm and the area of the top electrodes is $6.2 \times 10^{-5}\,\text{cm}^2$. Figure 7 shows the obtained hysteresis loops, which indicate that the polarization of the PZT film is saturated at 9 V and that the remnant polarization (P_r) was $30\,\mu\text{C/cm}^2$. When the polarization direction was downward [Fig. 1(b)], the measured polarization was sufficient for depleting all the electrons across the 30-nm-thick ZnO film, whose area density of intrinsic charge was calculated to be as low as $0.0005\,\mu\text{C/cm}^2$. When the polarization direction was upward [Fig. 1(a)], on the other hand, the polarization accumulated charges in the ZnO film with an area density of $30\,\mu\text{C/cm}^2$, which is larger than the intrinsic charge density by 6×10^4. Because the number of electrons in the depletion state is smaller than that of intrinsic charges, the ratio of the charge modulation induced by the polarization switching is larger than 6×10^4. Thus, we can expect a high I_{on}/I_{off} ratio of more than 6×10^4 for a FeFET containing the 30 nm ZnO/PZT/SRO structure.

C–V measurements revealed the charge response of the Pt/Ti/ZnO/PZT/SRO capacitor against the applied voltage [Fig. 8(a)]. We also characterized a Pt/Ti/PZT/SRO capacitor as a reference [Fig. 8(b)]. When a positive voltage was applied to the SRO electrode, the capacitance of the Pt/Ti/ZnO/PZT/SRO structure was similar to that of the Pt/Ti/PZT/SRO structure. This result indicates that quasi-two-dimensional electrons are accumulated at the ZnO/PZT interface, because the ZnO film has no contribution to the total capacitance in a series. When negative voltages were applied to the SRO electrode, in contrast, the total capacitance was reduced as a result of the full depletion of the 30 nm ZnO film. These accumulation and depletion states in the ZnO film were preserved even when the applied voltage was removed.

The I_{ds}–V_{gs} characteristics of a FeFET with the Pt/Ti/ZnO/PZT/SRO structure was measured at $V_{ds} = 0.1\,\text{V}$ and

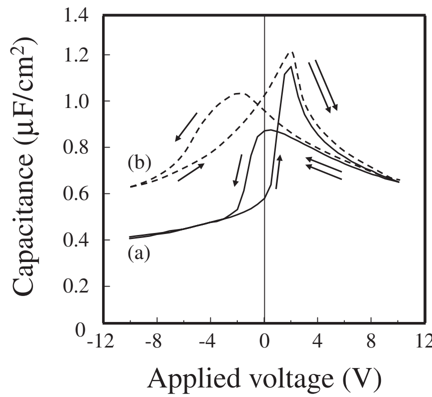

Fig. 8. C–V characteristics of (a) Pt/Ti/ZnO/PZT/SRO (solid line) and (b) Pt/Ti/PZT/SRO (dotted line) capacitors.

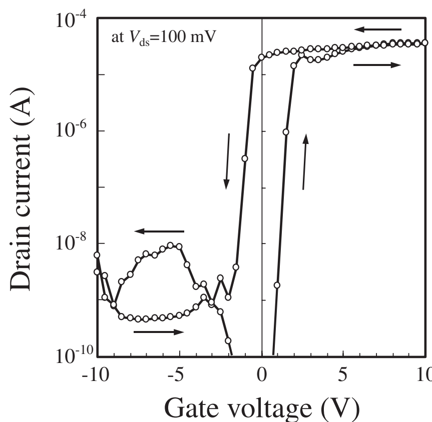

Fig. 9. I_{ds}–V_{gs} characteristics of FeFET with 30-nm-thick ZnO film.

are shown in Fig. 9. The drain current shows a counter-clockwise hysteresis loop, corresponding to the ferroelectric polarization switching, and eventually splits by five orders of magnitude when the bias voltage is cycled between -10 and $+10$ V, according to the accumulation ($V_{gs} > 0$) and depletion ($V_{gs} < 0$) of the ZnO film. The ratio of the drain currents higher than 10^5 approximately corresponds to the calculated ratio of the charge modulation in the 30 nm ZnO film between the accumulation and the depletion. The split of the on and off states remains when the gate voltage is returned to zero. Furthermore, the midpoint of the subthreshold swings is very close to a zero bias, which suggests that the amount of space charge in the PZT film and at the ZnO/PZT interface is markedly low, as anticipated from the structural characterization. Therefore, a good retention property can be expected for the fabricated FeFET.

We investigated the retention characteristics of the fabricated FeFET at room temperature without applying a gate voltage during the retention periods. First, as an initial write (on state) operation, a FeFET was biased with $V_{gs} = 10$ V and $V_{ds} = 0$ V for 500 ns. Then, the device state was probed by drain current measurements as a function of retention time under a bias condition of $V_{ds} = 0.1$ V and $V_{gs} = 0$ V. Similarly, an off-state retention was characterized by first biasing the FeFET at $V_{gs} = -10$ V and $V_{ds} = 0$ V for 500 ns and then measuring the drain currents with the same bias condition of $V_{ds} = 0.1$ V and $V_{gs} = 0$ V. As can be seen

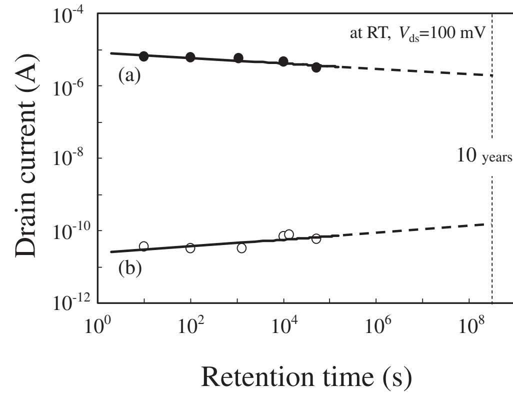

Fig. 10. Retention characteristics of FeFET for (a) on state and (b) off state.

in Fig. 10, no significant change in the drain current was observed in the both states during the retention tests. As a result, the I_{on}/I_{off} ratio was initially 10^5 and it was greater than 10^4 even after 10^5 s. An extrapolation of the retention behavior predicts a definite memory window of over ten years.

The stable on and off states are expected from physical insights of the Pt/Ti/ZnO/PZT/SRO structure. In the on state, electrons in the ZnO film strongly coupled with the polarization of the PZT film are accumulated at the ZnO/PZT interface under a flat-band condition inside the PZT layer. On the other hand, because the electron density of the ZnO layer is low enough, the conductivity of the fully depleted ZnO layer is extremely low in the off state. Thus, a high I_{on}/I_{off} ratio can be maintained for a long time.

4. Conclusions

We have developed a ferroelectric-gate field-effect transistor containing a heteroepitaxially stacked nonpolar-ZnO/PZT/SRO/STO structure. An electron gas accumulation and complete depletion switching operation has been carried out by using an ultrathin nonpolar ZnO film with an extremely low carrier density ($\sim 10^{15}$ cm^{-3}). As a result, a high on/off ratio of drain current of more than 10^5 was realized. Furthermore, a long retention time, longer than 10^5 s, with an on/off ratio of 10^4 was achieved.

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