Studies on Electrical Properties of Integrated Ferroelectric Capacitors and Their Degradation Processes

YASUHIRO SHIMADA

2003
SYNOPSIS

Although the concept for the use of ferroelectric materials in semiconductor devices was proposed about 30 years ago, ferroelectric memories had not become a commercial reality until the late 1980s due to premature ferroelectric thin film technologies. The first demonstration of a ferroelectric random access memory (FeRAM) was made in 1987 and the subsequent discovery of fatigue-free ferroelectric materials in 1992 has proved the validity of these materials for FeRAMs with high read/write endurance. These demonstrations stimulated a great deal of effort to realize practical high-density FeRAMs. Since then, the incorporation of ferroelectric materials into integrated circuits has been booming across the semiconductor industry, being supported by the projection to replace conventional nonvolatile memories with FeRAMs rapidly. Meanwhile, crucial demands for the use of high-dielectric-constant materials in dynamic random access memories (DRAMs) arose from the need for extension of the DRAM density along the trend in the scaling of device structures, as existing technologies based on traditional capacitor dielectrics were approaching their certain unavoidable physical limitations on building high-density DRAMs. Contrary to these growing expectations, ferroelectric memories were first introduced in limited applications and they have not evolved into a major manufacturing segment of semiconductor industry yet. One of the dominant reasons is that ferroelectric memories are still certainly plagued with unsolved reliability problems including time-dependent dielectric breakdown (TDDB), leakage current instability, read/write endurance, charge retention, and imprint in integrated ferroelectric capacitors. These subjects are not only important to device engineering but also fairly interesting as fundamentals in ferroelectric and semiconductor physics. It is therefore informative and beneficial for us to reach correct understandings of underlying mechanisms through more intensive studies on electrical degradation processes in integrated ferroelectric capacitors and thereby to establish confident reliability models for ferroelectric memories.

In this thesis the author intends to explain the majority of electrical degradations in
ferroelectric capacitors in terms of the motion of charge carriers. Detailed experimental investigations on the changes in electrical properties of integrated ferroelectric capacitors under various electric field and temperature conditions are carried out to reveal their degradation mechanisms. Accordingly the discussion of electrical degradation mechanisms takes up the major part of this thesis with meaningful electrical and reliability data obtained from experimental observations. Throughout a systematic study of the electrical degradation phenomena, the emphasis is placed on the presence of mobile ions, such as ionized oxygen vacancies distributed at deep levels (\( \sim 1 \text{ eV} \)) in the energy bandgap, and electrons and holes related to defects with activation energies in the range of 0.2 - 0.4 eV, whose motion would cause a change in the distribution of space charge in the ferroelectric capacitor, resulting in a variety of failures in ferroelectric memories over a long period of time.

This thesis is organized with the following chapters. A brief review of recent progress in ferroelectric memory technologies is given in Chapter 1. Subsequently, recent achievements in materials and processing technologies that can improve the reliability performance of DRAMs and FeRAMs incorporating ferroelectric capacitors are overviewed in Chapter 2. Chapters 3 and 4 are related to leakage current issues in integrated barium-strontium titanate (Ba\(_{1-x}\)Sr\(_x\)TiO\(_3\); BST) capacitors applicable to high-density DRAMs. The temperature and voltage dependencies of the leakage current in integrated BST capacitors are characterized in Chapter 3. Possible mechanisms dominating the electrical conduction under the considered temperature and voltage conditions are discussed. Chapter 4 deals with the resistance degradation issue of the integrated BST capacitors under temperature and voltage stresses. The time-dependent leakage current behaviors are studied for two types of samples obtained from different film growth processes. The current-voltage analysis reveals a dominant conduction mechanism causing an increase in leakage current in the presence of excess temperature and voltage stresses. Chapters 5, 6, and 7 deal with the integrity of ferroelectricity during the shelf-life of ferroelectric capacitors fabricated from strontium bismuth tantalate-niobate (SrBi\(_2\)(Ta,Nb)\(_2\)O\(_9\); SBTN) for FeRAM applications. In Chapter 5,
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1.1 FERROELECTRICS IN SEMICONDUCTOR MEMORIES

Ferroelectric materials applicable to semiconductor memory devices, in general, are characterized in terms of two of the most important electrical properties; (1) high-dielectric constant and (2) spontaneous polarization. These fundamental properties are exploited in two different types of memories, volatile and nonvolatile memories, to lower the barriers for the two different technical challenges that traditional semiconductor memories are facing:

First, there is a physical limitation on the thickness of traditional capacitor dielectrics, such as silicon dioxide (SiO₂) or silicon nitride (Si₃N₄), used in high-density dynamic random access memories (DRAMs). In a DRAM cell a binary datum is represented by a certain amount of electric charge stored in a storage capacitor. To minimize the area occupied by the cell, minimization of the area occupied by the storage capacitor is required. To reduce the capacitor area without reducing the capacitance per unit area, a reduction in the thickness is required. Even if deep-trench or three-dimensional structures are used for extending the effective capacitor area within a limited cell area, the thickness of such traditional capacitor dielectrics with relatively low dielectric constants is required to be less than a few nanometers in the multimegabit DRAM generation and beyond. This region is far below the realistic thickness of the dielectrics with confident reliability. High-dielectric-constant materials, on the other hand, can provide a relatively large capacitance per unit area with a realistic thickness, so that it is an attractive choice to replace the traditional capacitor dielectrics with these high-dielectric-constant materials.
for simplification of the cell structure.1-6)

Second, recent strong demands for lowering the power dissipation of portable computers and mobile communication devices have given rise to a crucial need for a nonvolatile memory with fast operation speed, low power consumption, unlimited read/write endurance, and long data retention. A ferroelectric capacitor can preserve information in terms of the bistable polarization, which can take a binary datum, “0” or “1”. The complementary polarization states are fairly stable against thermal disturbance under no electric field and are readily switched from one state to the other by flipping the polarization in the direction of a low applied electric field. These specific electrical properties of ferroelectrics lead to an anticipation that ferroelectric random access memories (FeRAMs) have potential advantages in the operation speed and operation voltage7,8) and therefore will accelerate the proliferation of FeRAMs as an alternative to traditional nonvolatile memories.

The following is a brief review of the historical progress in ferroelectric technologies for high-density DRAMs and FeRAMs. Table 1 shows remarkable achievements in the field of ferroelectric memory technologies.

The high-dielectric-constant nature of ferroelectrics originates from a large displacement of cations against the negatively charged oxygen surroundings in the perovskite structure under an applied field.9) These materials exhibit the values of dielectric constants in the range from 200 to 1000 in the paraelectric phase at room temperature even if these materials are prepared in thin films. In the early 1990s, some of the ferroelectric materials have been found to be useful in high-density DRAMs and compatible with advanced complementary metal-oxide-semiconductor (CMOS) memory processing, as a result of a rapid progress in the thin film technology.10-13) In particular, barium-strontium titanate (Ba1-xSrₓTiO₃; BST), barium titanate (BaTiO₃; BTO), and strontium titanate (SrTiO₃; STO) have been investigated for use as capacitor dielectrics.

Unlike the capacitor using SiO₂, however, reliability of the capacitors using high-dielectric-constant materials is not only dominated by catastrophic breakdown after a long period of time but also by a gradual increase in leakage current during the operation.
Table 1.1  Historical achievements in the field of ferroelectric technologies.

<table>
<thead>
<tr>
<th>Nonvolatile Memory</th>
<th>Volatile Memory</th>
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<tbody>
<tr>
<td>Non-Destructive Readout</td>
<td>Destructive Readout</td>
</tr>
<tr>
<td>1963 Moll et al., Modulation of FET conductance</td>
<td>1994 Sumi et al., 256Kb (SBT)</td>
</tr>
<tr>
<td>1974 Wu, MFS FET operation</td>
<td>1992 Fijii et al., eq. t1.3nm (BST)</td>
</tr>
<tr>
<td>Progress in thin film technology (MOD, sol-gel, sputter, CVD)</td>
<td>1990 Kinny et al., 512b (PZT)</td>
</tr>
<tr>
<td>1988 Eton et al., 256b (PZT)</td>
<td>1994 Eton et al., 256Kb (SBT)</td>
</tr>
<tr>
<td>Bismuth-layered perovskite (1992)</td>
<td>1995 Nakamura et al., MFMIS (SBT)</td>
</tr>
<tr>
<td>IrOx electrode (1994)</td>
<td>1992 Fujii et al., eq. 1.3nm (BST)</td>
</tr>
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</table>

*eq. 1.3 nm means that the dielectric film has an SiO2 equivalent thickness of 1.3 nm.

Since the leakage current is the cause of charge loss of the capacitor during an interval of refresh cycles, it should be smaller than $10^{-5}$ A/cm$^2$, for instance, to maintain a charge loss of less than 10% in one second of a capacitor with an area of 0.01 $\mu$m$^2$ for lithographic feature sizes below 0.15 $\mu$m. Thus the lowering of leakage current and its stabilization during the operational life are the major challenges for realizing future high-density DRAMs using high-dielectric-constant materials.

Despite the excessive expectation of a close advent of such high-density DRAMs, the use of ferroelectric materials was firstly encouraged by commercialization of a series of BST-capacitor-embedded GaAs microwave-monolithic integrated circuits (MMICs). Subsequently, the process compatibility of integrated BST capacitors with CMOS devices has also been proved in a video signal processor. High-density memory cell technologies using these high-dielectric-constant materials for gigabit DRAM generations are still under intensive development.

Ferroelectric materials such as lead-zirconium titanate (PbZr$_x$Ti$_{1-x}$O$_3$; PZT) and
strontium bismuth tantalate-niobate (SrBi$_2$(Ta,Nb)$_2$O$_9$; SBTN), on the other hand, are of great importance in nonvolatile memory applications because these materials can be prepared in thin films and maintain an induced polarization even after the removal of the poling field.\textsuperscript{17} In addition, ferroelectric capacitors are readily implemented onto a CMOS wafer by adding an optional process after the completion of underlying CMOS transistor processing. Typical FeRAMs use a one-transistor and one-capacitor (1T/1C) cell structure, which are commonly used in DRAMs, or a two-transistor and two-capacitor (2T/2C) cell structure, which is more stable in operation than the 1T/1C cell structure whereas the cell size is doubled. As a more advanced class of FeRAMs, ferroelectric-gate transistor devices have been proposed. These device structures are similar to those of floating-gates in erasable and programmable read-only memories (EPROMs) or electrically erasable and programmable read-only memories (EEPROMs), where the gate is stacked either in a metal-ferroelectric-semiconductor (MFS) structure,\textsuperscript{18} in a metal-ferroelectric-insulator-semiconductor (MFIS) structure, or in a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure,\textsuperscript{19} with which the conductance of the semiconductor channel under the gate is modulated.

Although the concept for the use of ferroelectric materials in nonvolatile memories was already proposed 30 years ago\textsuperscript{20} and many researchers had tried to incorporate the ferroelectric materials into those devices, integrated ferroelectrics did not become a commercial reality until ferroelectric thin film technologies matured in the late 1980s. Beginning with the first demonstration of a ferroelectric memory by Krysalis Microelectronics in 1987,\textsuperscript{21} some of ferroelectric memories using PZT in 2T/2C cells have been commercialized to date.

The operation principles of ferroelectric memories using the 1T/1C or 2T/2C cell structure are quite similar to those of DRAMs. The simple cell structures ensure further minimization of the area occupied by the memory cell with the aid of advanced semiconductor process technologies. In addition, the fast switching time on polarization reversal within 200 ns and the low coercive field below 100 kV/cm will procure the high-speed and low-voltage operation of FeRAMs. In these regards, FeRAMs have been
accepted as an attractive alternative to traditional nonvolatile memories such as EEPROMs or Flash memories (flash-EEPROMs).

Ferroelectric materials for FeRAMs studied in early works have primarily been limited to PZT because of its high remanent polarization in thin films. However there was a critical issue of electrical degradation in PZT, ferroelectric fatigue, which can be defined as the loss of switchable polarization with repeated hysteresis cycling. Later on the fatigue of PZT was attributed to accumulation of oxygen deficiency at the platinum (Pt) electrode interface from the fact that the fatigue of PZT was significantly suppressed by replacing metallic Pt electrodes with oxide electrodes such as (La,Sr)CoO₃ (LSCO), RuO₂, and IrO₂.

Following the electrode interface engineering, a breakthrough discovery of fatigue-free ferroelectric materials has been made by Symetrix group in 1992. This achievement has expanded the ferroelectric memory applications as replacements for SRAMs as well as EEPROMs. The innovative materials belong to a bismuth-layered perovskite family of materials, such as SrBi₂Ta₂O₉ (SBT) and SrBi₂(Ta,Nb)₂O₉ (SBTN). Although bismuth-layered perovskites exhibit relatively smaller polarization than PZT, these materials have demonstrated extremely low fatigue in polarization even with the use of Pt electrodes. The first demonstration of a read/write operation of more than \(10^{12}\) cycles was made in an experimentally fabricated 256-kbit FeRAM using one of the bismuth-layered perovskites, SBT. Since then, engineering of these fatigue-free materials has been focused on the controlling of their reliability-related properties such as leakage current, retention, and imprint.

### 1.2 PROBLEMS IN FERROELECTRIC MEMORIES

In spite of the prediction of rapid replacements of traditional capacitor dielectrics with high-dielectric-constant materials and also of existing nonvolatile memories with FeRAMs, ferroelectric memories have not evolved yet to be a major manufacturing segment of semiconductor industry because these materials are still certainly plagued with
reliability issues associated with electrical degradations such as time-dependent dielectric breakdown (TDDB), resistance degradation, read/write endurance, charge retention, and imprint. Unfortunately most of these critical issues still remain unsolved. Therefore we need fundamental understandings of electrical degradation mechanisms in the ferroelectric materials for further improvements in the reliability of ferroelectric memories required from a practical point of view as well as from an academic point of view.

Reliability of integrated ferroelectric memories, in general, primarily depends on the electrical integrity of the ferroelectric capacitors used. Accordingly the quality of ferroelectric thin films determined at the growth process during crystallization has a great impact on the reliability of ferroelectric memories. In addition, the reliability of ferroelectric memories is readily infected with the subsequent back-end semiconductor integration processes such as plasma etching, film deposition by sputtering and/or CVD, and forming in $H_2^{32-36}$ even if the ferroelectric films were successfully grown. Circuit design considerations are also required to lower the susceptibility of ferroelectric memories to possible failure mechanisms through the incorporation of margins in the driving circuits, the application of redundancy, fault tolerance, and other reliability enhancement techniques. For instance, circuit designers should take care of the electrical durability of ferroelectrics, such as variations in switchable charge and in coercive voltage, to procure the stable and reliable memory performance. In this regard, we can describe the reliability of ferroelectric memories as a function of the materials, processes, and circuit design techniques used. Finally, the reliability of ferroelectric memories is assured as consequences of proper screening, sampling for failures, life testing, application of field use data, and further improvements by taking corrective actions at all levels through design and manufacturing.

As noticed from the above argument, improvements in ferroelectric memory performances are often carried out effectively by considering the reliability data, which are interpreted properly based on confident degradation models which well describe the related memory failures. However, memory failures are caused by a variety of electrical degradation mechanisms in ferroelectric capacitors. For instance, resistance degradation,
time-zero dielectric breakdown, and TDDB are the most critical reliability limiting factors of high-density DRAMs fabricated from high-dielectric-constant materials. In addition, retention and endurance are generic requirements for FeRAMs. Therefore we need a comprehensive understanding of the relationship between ferroelectric degradation phenomena and use conditions, in other words, the knowledge of acceleration factors, which are valid for saving required time for qualification of ferroelectric memories. As ferroelectric memories find their way in future electronic applications as replacements for traditional DRAMs, EEPROMs, SRAMs, and so on, correct understandings and proper models of the failure mechanisms will be the most important basis for confident reliability assessment.

1.3 SCOPE AND ORGANIZATION

As described above, the reliability of ferroelectric memories and the electrical behavior of ferroelectric capacitors are intimately related each other. In addition, it seems that most of the electrical degradation mechanisms are linked with each other through an underlying physical process. The principal purpose of this work is to unravel the underlying mechanisms of electrical failures in high-density DRAMs and nonvolatile FeRAMs arising from allied electrical degradation and aging effects in integrated ferroelectric capacitors. Based on these mechanisms, the author attempts to establish confident reliability models that can predict the performance of ferroelectric memories under given environmental and operating conditions and to provide essential and meaningful feedback for ferroelectric materials, circuit design, and manufacturing process improvements.

This thesis is organized into eight chapters. Following this introductory chapter, advanced materials and process technologies required for reliable ferroelectric memory performance are overviewed in Chapter 2. Chapters 3 and 4 are related to leakage current issues in integrated BST capacitors. The temperature and voltage dependence of the leakage current in integrated BST capacitors is characterized in Chapter 3. In view of
carrier transport in semiconductive dielectrics, relevant mechanisms dominating the electrical conduction under temperature and voltage conditions considered are discussed. Chapter 4 deals with the resistance degradation issue of the integrated BST capacitors under temperature and voltage stresses. The time variation in leakage current is studied for two types of samples fabricated through different film growth processes. The current-voltage ($J-V$) analysis reveals a dominant conduction mechanism causing an increase in leakage current in the presence of excess temperature and voltage stresses. Chapters 5 through 7 deal with nonvolatile ferroelectric materials and their specific issues related to the integrity of ferroelectricity during the shelf-life. In Chapter 5, temperature effects on charge retention characteristics of integrated SBTN capacitors are studied. It is shown that the loss of remanent polarization is primarily due to the instantaneous relaxation as a function of temperature. Stability of remanent polarization for subsequent storage at high temperatures is discussed. Chapter 6 describes retention failures in a 288-bit ferroelectric memory using SBTN. A statistical distribution analysis of retention failures leads to empirical failure models that can predict the retention performance including the contributions from infant failures and random failures. In Chapter 7, thermally induced imprint in ferroelectric SrBi$_2$(Ta,Nb)$_2$O$_9$ capacitors is investigated by storing poled capacitors at high temperatures. The change in the switchable polarization is ascribed to redistribution of electrons during the thermal aging process. Finally, Chapter 8 summarizes the results obtained throughout this work together with a prospect for future extension of this kind of studies and their impact on the emerging ferroelectric memory devices.

To give an alternative perspective of this work, a schematic chart of systematic development of ferroelectric memories segmented into typical feedback processes before product release is illustrated in Fig. 1.1. General reliability limiting factors in ferroelectric memories are figured out with the corresponding chapter number(s) in which related ferroelectric properties and underlying mechanisms are studied.
Fig. 1.1  A feedback process flow for systematic development of ferroelectric memory devices, emphasizing effective improvements in the leading-edge ferroelectric technology by understanding degradation mechanisms of ferroelectric capacitors. Reliability limiting factors to be considered are typed out with the corresponding chapter number(s) in which related mechanisms are discussed.
2.1 INTRODUCTION

High-dielectric-constant ferroelectric materials such as BST can be used as a capacitor dielectric in high-density DRAMs to accumulate a sufficient amount of charge to provide a logic signal in a small area of the memory cell.\textsuperscript{2-6} In contrast ferroelectric materials exhibiting the spontaneous polarization can be used to storage binary bits of information, “0”s and “1”s, corresponding to the two definite remanent polarization states.\textsuperscript{7,8} For the last three decades, both of these ferroelectric materials have been considered to be vital materials to fulfill electrical requirements from future semiconductor memories mainly made of silicon. In recent years, integration of ferroelectric materials into semiconductor memories has been made successfully.\textsuperscript{10-13} This innovation in semiconductor memories was brought about by great advances in the ferroelectric thin film technology in the late 1980s, including sol-gel, sputtering, and dry etch techniques, resulting in high quality ferroelectric films implemented in semiconductor devices. Since then, great efforts have been increased to develop and establish state-of-the-art integration processes for high-density and nonvolatile ferroelectric memories.

The author has also been engaged in various film and integration technologies applicable to ferroelectric memories. First of all, a liquid source misted chemical deposition (LSMCD) technique using MOD liquid precursors for ferroelectric film preparation was introduced to form conformal ferroelectric thin films on microsteps or microtrenches.\textsuperscript{37-39} Subsequently, an effective dry etching technique for Pt electrode patterning was developed.\textsuperscript{13} Since the etch rate of Pt was drastically increased in the...
presence of chlorine additive to rare-gas plasma, evaporation of platinum chlorides assisted by energetic ion bombardment is proposed as a possible etching mechanism.\textsuperscript{40}) Finally, TiN diffusion barriers were introduced at the interface of Pt/Al or Pt/poly-Si interconnects to prevent the diffusion-induced reaction at the electrical contacts.\textsuperscript{10}) Using these advanced process technologies, several ferroelectric test vehicles such as high-density DRAMs and nonvolatile FeRAMs have been fabricated to date. These ferroelectric memories have potential advantages in cell size, speed, power, endurance, and so on, with respect to traditional semiconductor memories. However, the performance and reliability are strongly dependent on the device structure and operating conditions. It is therefore preferable to understand the basic device structures and operating principles before studying the detailed ferroelectric device physics.

This chapter reviews typical ferroelectric memory cell structures and the operating principles in accordance with the materials used. A novel circuit technology will be proposed to challenge FeRAM-embedded systems-on-chips. Subsequently, advanced ferroelectric integration technologies and their issues are described. Finally, fundamentals in electrical properties which govern the reliability of integrated ferroelectric capacitors, such as leakage current, TDDB, and ferroelectric fatigue in polarization, are discussed.

### 2.2 DRAMs USING HIGH-DIELECTRIC-CONSTANT MATERIALS

As stated by Moore’s law, the memory density of DRAMs has increased by a factor of 4 every three years during the past 25 years. For future DRAMs, for instance, the area available for the storage capacitor in a DRAM cell is decreased by a factor of 10 as the lithographic feature size, defined by metal half-pitch, decreases from 0.25 to 0.10 μm. The minimum amount of charge to be preserved in the storage capacitor, however, is determined by the sensitivity limit of the sense amplifier, parasitic capacitances, and influence of alpha-particles. Although the minimum amount of charge has empirically decreased by about a third per generation and is expected to be decreasing continuously at
the same rate, a similar decrease in operating voltage is also expected for future generations. Consequently, the storage capacitor continues to require a nearly constant capacitance of 25 – 30 fF. Accordingly, as the feature size decreases, DRAM cells need to be shrunk on a smaller silicon surface area while keeping the capacitance constant. If the miniaturization of storage capacitors using silicon dioxide (SiO$_2$) is continued by making the SiO$_2$ layer thinner with extending the effective surface area on three-dimensional trench or fin structures, the SiO$_2$ film in future DRAMs will eventually be thinner than that of tunneling gates ( < 10 nm ). For instance, the thickness of SiO$_2$ film required to provide a capacitance of 30 fF within a surface area of 0.01 $\mu$m$^2$ is calculated to be 0.01 nm, which is thinner than the thickness of a mono-atomic layer of SiO$_2$. In addition, the increased surface area will lead to an increase in production cost due to the complexity. Therefore the limitation on the thickness of traditional capacitor dielectrics leads us to another choice of materials which can provide a higher capacitance for high-density DRAMs.

To use high-dielectric-constant materials, including ferroelectric materials, is such a choice to increase the capacitance of the storage capacitor. High-dielectric-constant ferroelectric materials such as Ba$_x$Sr$_{1-x}$TiO$_3$ (BST) and SrTiO$_3$ (STO) can offer a desirable capacitance with a thickness of a few hundred nanometers, which can not be attained with the traditional capacitor dielectrics. In high-density DRAM cell structures, the traditional capacitor dielectrics can be replaced simply with the high-dielectric-constant materials. With a proper choice of cell/bit-line capacitance ratio, the memory cell structure of such ferroelectric DRAMs becomes quite similar to those of existing DRAMs, i.e., a simple combination of one transistor and one capacitor (1T/1C). An equivalent circuit of a 1T/1C memory cell for DRAMs and the cell structure are shown in Fig. 2.1.

2.3 NONVOLATILE FERROELECTRIC MEMORIES

A memory capacitor using a ferroelectric material has bistable polarization states in the polarization versus voltage ($P$–$V$) hysteresis loop at $V = 0$, as shown in Fig. 2.2(a). In
Fig. 2.1  A one-transistor and one-capacitor (1T/1C) ferroelectric memory cell structure.

In this figure, the up and down states are assigned to logic “1” and logic “0”, respectively. When the applied field across the ferroelectric capacitor exceeds a critical field, called a coercive field, the polarization is switched and aligned along the applied field (Fig. 2.2(b)). The coercive field is typically ranging from 50 to 100 kV/cm depending on chemicals and preparation conditions of ferroelectric thin films, so that the switching voltage of the ferroelectric capacitor with the film thickness in the range of 100 – 200 nm is in the range of 0.5 – 2 V. These low switching voltages allow the capacitor to preserve binary information denoted by either “0” or “1”, according to the direction of the switched polarization with a standard supply voltage of less than 5 V. In addition, the stored information is maintained for a very long period of time without supplying a power due to the remanence of a finite polarization in the absence of field. The polarization at zero bias is coupled to the same amount of free charge on the capacitor plate, typically a few tens of microcoulombs per
Fig. 2.2  Polarization of a ferroelectric capacitor as a response (a) to the applied voltage, resulting in the up (logic “1”) or down (logic “0”) state on the hysteresis loop at zero bias, and (b) to the applied field along which cations shift from equilibrium positions to the others.

square centimeter (μC/cm²), which will be sensed as a bit-line signal when a read pulse is applied.

Figure 2.3 compares two memory cell configurations. The two-transistor and two-capacitor (2T/2C) cell configuration has been the major architecture of choice for nonvolatile ferroelectric memories.\textsuperscript{21-23} In this configuration, the readout operation is quite stable because a pair of 1T/1C elements in the 2T/2C cell hold complementary data corresponding to the two definite logic states. For high-density memories, however, a simpler cell structure such as 1T/1C is preferable.\textsuperscript{31} The 1T/1C cell structure allows 1 gigabits for scaling of nonvolatile ferroelectric memories if the capacitor area of less than 0.2 μm² is available. In the case of the 1T/1C configuration, the bit-line voltage is
Fig. 2.3 Ferroelectric memory cell architectures: (a) two-transistor and two-capacitor (2T/2C) cell, and (b) one-transistor and one-capacitor (1T/1C) cell. BL: bit-line, WL: word-line, CP: cell plate, and S.A.: sense amplifier.

determined by the transferred charge from a selected cell capacitor, which is subsequently compared with a certain reference voltage to discriminate the logic state of stored information. The reference voltage is generated from an additional circuit involving a reference cell.

2.4 EMBEDDED FeRAMs

Systems-on-chips are integrating more functions with the increment of both the operation speed and packing density. Contactless integrated circuit (IC) cards are such leading-edge products for identification and electronic commerce. As demonstrated in experimentally fabricated logic and microcontroller large scale integrated circuits (LSIs), FeRAM is the best choice for the nonvolatile memory to be incorporated in
such LSIs because of its advantages in read/write speed and operation power as well as in read/write endurance. A typical map of operational power supply voltage versus access time for an experimentally fabricated 256-kbit FeRAM using SrBi$_2$Ta$_2$O$_9$ (SBT) is shown in Fig. 2.4.\textsuperscript{31) } The SBT-based FeRAM ensures the fast access time ($< 200$ ns) at low operation voltages ($< 3$ V).

In contactless IC card applications, several radio frequency (RF) demodulation schemes are used. Due to the superior noise immunity, low carrier frequencies, e.g., 125 kHz, are used for low data transmission rate applications ($\sim$10 kbps), while the card requires a coiled antenna in many turns with an additional coupling capacitor. Since the
size of data to be transmitted was small enough for early identification applications, a 288-bit FeRAM fabricated from SBT had been incorporated in a logic LSI operating at 125 kHz and 7.8 kbps by binary phase shift keying (BPSK).  

For high data transmission rate applications higher carrier frequencies are preferred, while the noise interference effect becomes significant as the carrier frequency is increased. Figure 2.5 shows a 1-kbit FeRAM-incorporated logic LSI developed for 13.56 MHz application. The die dimensions are $1.8 \times 2.5 \text{ mm}^2$ and the thickness is reduced to 180 $\mu\text{m}$ for use in 700-$\mu\text{m}$-thick contactless IC cards. The system is comprised of an analog front-end (a power generator, power-on reset, clock generator, modulator, and so

![Fig. 2.5](image_url)
forth), a control logic, and a 1-kbit FeRAM module. The power generation circuitry generates the DC supply voltage by rectifying the 13.56-MHz power signal received with a tuned resonant circuit connected to the LSI. The data packet is transmitted from a reader/writer unit at a rate of 212 kbps modulated on the power signal by amplitude shift keying (ASK). The LSI responds to the inquiry from the reader/writer unit at the same data transmission rate using binary phase shift keying (BPSK) modulation at 848 kHz. This product is fabricated with a single-metal, single-poly and 0.8-μm CMOS technology.\textsuperscript{13}

In advanced contactless IC cards for electronic commerce, the highest levels of security are of necessity. One of the effective solutions to this problem is the use of systems-on-chips involving a microcontroller unit (MCU) with a captive logic or co-processor capable of cryptographic data processing. The latest commutation IC card uses an 8-bit MPU-embedded LSI with a 14-kbit FeRAM provided with a double metal, single-poly and 0.6-μm CMOS technology. The LSI has a cryptography logic circuitry based on the data encryption standard (DES) and can address anti-collisional communications among neighboring cards. The carrier frequency is 13.56 MHz and the communication protocol follows the ISO14443 regulation. The IC card can reach the reader/writer unit from 10 cm away.

More advanced systems-on-chips may incorporate reconfigurable logic arrays, instead of captive co-processors, to address many different algorithms for cryptographic data processing. However it takes a time to reconfigure all of the separated logic blocks one after another. To save the undesirable reconfiguration time, a distributed logic array architecture with many local array elements was proposed (Fig.2.6).\textsuperscript{44} In this architecture, each array element has an FeRAM which holds logic circuit patterns of itself. When a reconfiguration command is executed, the logic in every element is changed simultaneously.

A low-power operation of FeRAMs is also achievable by introducing a multi-mode memory operation, according to the system status.\textsuperscript{44} When the system is working, every data in the FeRAM is considered to be temporal. This allows a small voltage amplitude for
Fig. 2.6  A distributed logic array architecture for fast reconfiguration.

Fig. 2.7  A multi-mode operation along (a) a minor hysteresis loop as a response to a small voltage amplitude applied to the capacitor to be used in a power save mode during the system is working and (b) a major hysteresis loop as a response to a large voltage amplitude applied to the capacitor to be used in a shut-down mode to restore the remanent polarization before the power is turned off.
storing a datum on the minor loop of the hysteresis and for saving the operating power (Fig.2.7(a)). When the system is being shut-down, every data is restored along the major loop of the hysteresis with a large voltage amplitude in order to secure the data retention (Fig.2.7(b)). Combining the low power and high speed FeRAM circuit techniques, it was calculated that the duration of a reconfiguration update is halved and the total power is saved by 30%.

2.5 FERROELECTRIC INTEGRATION TECHNOLOGIES

2.5.1 Process Integration

Reliability of integrated ferroelectric capacitors is strongly dependent on the wafer fabrication processing. First of all, high-quality ferroelectric thin films must be grown on the electrode plate. Any defects, imperfect crystallinity, or off-stoichiometry induced in the films during wafer fabrication processing are sure to cause an increase in leakage current, low dielectric constant, and/or poor ferroelectricity. Second, optimum choices and combinations of ferroelectric materials, electrode materials, and insulating materials are of necessity to ensure the reliability of integrated ferroelectric capacitors. Finally, even though the ferroelectric materials exhibit intended electrical properties after the film growth process, it is more important that those properties can be maintained and controlled throughout the entire fabrication process. These integration issues certainly arise from the incompatibility of ferroelectric materials with silicon process technologies. For instance, there are many sources of damage in ferroelectric processing, such as forming, annealing, and plasma etching. In this section, we will discuss key techniques enabling the integration of ferroelectric capacitors into silicon devices.

2.5.2 Film Deposition Techniques

The metal-organic decomposition (MOD) technique is preferable for growing ferroelectric thin films for low density device applications because of their simple device structure with a film thickness of typically 150 – 200 nm. Figure 2.8 shows a schematic
A schematic flow of metal-organic decomposition (MOD) of a Ba$_{1-x}$Sr$_x$TiO$_3$ solution.

Fig. 2.8 A schematic flow of metal-organic decomposition (MOD) of a Ba$_{1-x}$Sr$_x$TiO$_3$ solution.

flow of a typical MOD technique. Ferroelectric thin films are deposited on the substrate by spin-on coating of a homogeneous solution containing stoichiometry correct precursors, followed by subsequent drying and annealing for crystallization. The spin-on technique allows for lowering the machine overhead for manufacturing the integrated ferroelectric devices as well as for obtaining stoichiometry correct films from liquid solutions. A typical result of this technique using a BST solution is shown in Fig. 2.9. The lattice constant of the BST thin films as a function of the strontium (Sr) concentration is almost the same as that of bulk ceramics. This result ensures that bulk ferroelectric properties can be obtained even in thin films.

Although the MOD spin-on technique can provide with excellent composition controllability, uniform ferroelectric films are obtained only on planar substrates and the thickness is limited to as thin as 100 nm. For higher density devices with fine and complicated cell structures, such as multi-megabit DRAMs and FeRAMs, the thickness of
ferroelectric films becomes less than 100 nm and then superior step-coverage conformity is required. To improve the step-coverage conformity without losing the advantages of the MOD technique, a liquid source misted chemical deposition (LSMCD) technique using similar MOD liquid precursors was introduced. A schematic diagram of the LSMCD machine is illustrated in Fig. 2.10. This technique allows for unlimited choice of liquid precursor materials and requires no further composition control during the deposition at room temperature. Therefore this technique is also applicable to bismuth-layered ferroelectrics for nonvolatile ferroelectric memories as well as to high-dielectric-constant materials for gigabit scale DRAMs. Recent improvements in the mist delivery system has brought about a formation of misted particles in finer size from octane-based MOD type SBT solution. Figure 2.11 shows a resultant SBT film

![Graph showing Lattice constants of bulk and thin film Ba_{1-x}Sr_xTiO_3 as a function of molar fraction of Sr.](image-url)
Fig. 2.10  A schematic diagram of the LSMCD machine.

Fig. 2.11  Ultra-thin SBT film formed on sub-micron trenches by LSMCD.
formed on trenches with sub-micron lines and spaces, whose feature size is applicable to megabit scale FeRAMs.

2.5.3 Patterning of Ferroelectric Capacitors

Since ferroelectric materials made of oxides of metals and the electrodes made of Pt are chemically stable, there is a crucial issue in obtaining fine patterns by chemical wet or dry etching. Although ion milling is one of the widely used patterning techniques, the high energy ion bombardment causes a serious damage to the underlying MOS transistors and forms nonvolatile Pt compound residue on sidewalls of the photoresist, resulting in the formation of fences on capacitors. In addition, uniform etching of capacitors within a required tolerance in dimension is difficult due to the poor etch selectivity to the underlying materials.

To obtain better etch selectivities of the ferroelectric to Pt and Pt to SiO₂ using magnetron reactive ion etching (RIE), a variety of halide mixtures were examined, and consequently some of chlorine-based mixtures were found to be effective in improving the etch selectivities. Figure 2.12 shows a cross sectional micrograph of a Pt/BST/Pt capacitor fabricated with an RIE tool, which demonstrates the highly selective RIE feature with no undercutting of the bottom Pt electrode and the SiO₂ underlayer. Both the Pt and BST etch rates are ranging from 50 to 100 nm/min. With a proper choice of process gases and etch conditions, the RIE technique will challenge the sub-half micron range (< 0.25 μm) in feature size required for megabit scale DRAM fabrication.

2.5.4 Diffusion Barrier

When BST thin film capacitors are integrated in planar stacked memory cells, silicon diffusion from the buried polysilicon plugs into Pt electrodes becomes considerable. The diffused silicon forms a thin SiOₓ layer with a low dielectric constant at the interface between the Pt electrode and BST film, resulting in a lowering of the effective capacitance. The suppression of the silicon diffusion has been made by inserting TiN/Ti layers between the Pt electrode and poly-Si plug. Figure 2.13 shows compositional distributions across
Fig. 2.12 A cross-sectional micrograph of a Pt/BST/Pt capacitor patterned by RIE on a silicon substrate with CMOS circuits.

Pt/Ti/poly-Si and Pt/TiN/Ti/poly-Si structures observed by Auger electron spectroscopy (AES). The two structures were annealed in oxygen at 750°C for 1 h. It is clearly seen from Fig. 2.13(a) that the silicon diffusion is effectively suppressed by the inserted TiN/Ti barrier layer.

2.6 FUNDAMENTAL PROPERTIES OF FERROELECTRICS

2.6.1 High-Dielectric-Constant Materials (BST)

Recent efforts toward the applications of spin-coated BST thin films to GaAs MMICs and bypass-capacitor-incorporated microcontrollers have proved their potential validities for signal processing applications as well as memory applications.\textsuperscript{11,12,14-16} A typical current-voltage ($J$–$V$) characteristic of a Ba$_{0.7}$Sr$_{0.3}$TiO$_3$ film with a thickness of 140 nm
Fig. 2.13  AES depth profiles across (a) Pt(150nm)/TiN(200nm)/Ti(60nm)/poly-Si and (b) Pt(150nm)/Ti(60nm)/poly-Si structures.

Fig. 2.14  Current-voltage characteristics of a Ba_{0.7}Sr_{0.3}TiO_3 film with a thickness of 140 nm.
prepared by using the spin-on technique are shown in Fig. 2.14. The leakage current in the BST film is $2 \times 10^{-8}$ A/cm$^2$ at 3.3V, which corresponds to a charge loss of 0.2 fC per second for a capacitor with an area of 1 $\mu$m$^2$. Because a typical refresh cycle in DRAMs is shorter than 100 ms, this charge loss caused from the leakage current is low enough to maintain the stored charge (~30 fC) during the refresh cycle. Thus BST is a promising material for high-density DRAM capacitor dielectrics.

Figure 2.15 shows the frequency dependence of the dielectric constant for BST capacitors prepared at different anneal temperatures. When BST is annealed at 600 – 800°C, the dielectric constant remains unchanged in the frequency range above 1 GHz without dielectric losses. The low dielectric losses stem from the absence of ferroelectricity in the BST thin films at room temperature. Accordingly, integrated BST capacitors are advantageous in high frequency applications as well as DRAM applications when compared with other dielectric materials such as silicon nitride.

**Fig. 2.15** Frequency dispersion of the dielectric constant of Ba$_{0.7}$Sr$_{0.3}$TiO$_3$ capacitors annealed at 600, 700, and 800°C in oxygen.
Figure 2.16 (a) shows a Weibull plot of failure times for BST capacitors integrated in a microcontroller. The film thickness of BST is 185 nm. The capacitors were subjected to different electric field stress conditions at 125°C. The time to 0.1-% cumulative failure is then expressed as a function of electric field strength. Since the shape parameter of the distribution, \( m \), is greater than unity, the failure mode of the integrated BST films is intrinsic, i.e., the failures occurred in the wear-out period. From Fig. 2.16 (b), an estimated lifetime to 0.1-% cumulative failure under a voltage stress of 5.5 V at 125°C is longer than 10 years, which ensures the reliable performance of the integrated BST capacitors.

### 2.6.2 Nonvolatile Material (SBT, SBTN)

Since the nonvolatility is essential for FeRAMs, the integrity of remanent polarization in ferroelectric capacitors must be maintained under given voltage and thermal stresses for an intended device life. The durability of remanent polarization with voltage cycling is characterized by fatigue. When PbZr\(_x\)Ti\(_{1-x}\)O\(_3\) (PZT) is used in nonvolatile ferroelectric memory capacitors, fatigue becomes so significant after billions of read/write cycles giving rise to unintended memory malfunction. In PZT capacitors, the presence of space charges at Pt electrode interfaces is believed to be responsible for fatigue.\(^{50,51}\) In order to mitigate the interface effect, several electrode materials have been examined. For instance, PZT films combined with conductive oxide electrodes such as RuO\(_2\), LaSrCoO\(_3\), and IrO\(_2\) were reported to exhibit no significant fatigue even after 10\(^{12}\) cycles.\(^{25-28}\) More recently, an outstanding breakthrough in designing the materials for FeRAMs has been made by considering the atomic level microstructure of ferroelectrics.\(^{29,30}\) These materials exhibit a lack of fatigue even with simple metal electrodes, such as Pt. The structure of these materials has the general formula of multilayer interstitial ferroelectric compounds:

\[
(Bi\_2O\_2)^{2+}(A\_{m-1}B\_mO\_{3m+1})^{2-},
\]

(2.1)

where metal ion \( A \) can be Ca\(^{2+}\), Sr\(^{2+}\), Ba\(^{2+}\), Pb\(^{2+}\), Bi\(^{3+}\), La\(^{3+}\), etc., and metal ion \( B \) can be...
Fig. 2.16  Time-dependent dielectric breakdown (TDBB) characteristics for integrated BST capacitors with a thickness of 185 nm at 125°C. (a) A Weibull distribution of cumulative failures vs. stress time. (b) Time to 0.1-% cumulative failure vs. reciprocal of field strength.
Ti$^{4+}$, Ta$^{5+}$, or Nb$^{5+}$. For $m = 2$, for instance, Bi$_2$O$_2$ layers are periodically alternated with perovskite-like SrTa$_2$O$_7$ layers with double oxygen octahedral units, as shown in Fig. 2.17. Thus $m$ is the number of octahedral units in between the Bi$_2$O$_2$ layers. The direction of the spontaneous polarization is parallel to the $a$–$b$ plane of the layers because this plane contains periodic O–B–O chains that are known to contribute to the spontaneous polarization in the perovskite structure. In contrast, there is no spontaneous polarization along the $c$-axis because of the lack of periodic symmetry in the O–B–O chain. The

**Fig. 2.17** Structure of the SrBi$_2$Ta$_2$O$_9$ unit cell.
periodic lattice parameters for stoichiometric SrBi$_2$Ta$_2$O$_9$ (SBT) are $a = 5.52237$ Å, $b = 5.52408$ Å, and $c = 25.02641$ Å, exhibiting an orthorhombic distortion.$^{52}$ The choice of Sr for the metal $A$ site is advantageous in suppressing the metal deficiency, which causes a degradation in ferroelectricity, compared to the use of volatile Pb in PZT. In addition, the stacked Bi$_2$O$_2$ layers can be an oxygen source for compensation of oxygen vacancies induced in perovskite-like octahedra, because the oxygen ions in the perovskite-like layers are much more stable than those in the Bi$_2$O$_2$ layers.$^{53}$ Thus oxygen vacancies generated in the perovskite-like layers to cause fatigue are readily exchanged with oxygen ions in the Bi$_2$O$_2$ layers.$^{54}$ Therefore the bismuth oxide materials, such as SBT, are hardly to degrade in ferroelectricity, characterized by remanent polarization and coercive field, even if the deoxidation of ferroelectric occurs under the influence of Pt electrodes.

Figure 2.18 compares remanent polarizations of SBT and PZT capacitors as a function of the number of voltage cycles. When Pt electrodes were used for both

![Graph showing remanent polarization after fatigue for SBT and PZT capacitors using Pt electrodes.](image-url)

**Fig. 2.18** Remanent polarization after fatigue for SBT and PZT capacitors using Pt electrodes.
capacitors, a fatigue-free read/write operation was demonstrated in the SBT capacitor for up to $10^{12}$ cycles at 10 MHz and 200 kV/cm. Figure 2.19 shows typical hysteresis loops of 100-nm thick SrBi$_{2}$Ta$_{2-x}$Nb$_{x}$O$_{9}$ (SBTN) capacitors measured at 2 V. The hysteresis characteristics are strongly dependent on the chemical composition. For $x = 0.5$, for instance, the remanent polarization is $10 \mu$C/cm$^2$ with a coercive voltage of less than 1 V.\textsuperscript{55} These results indicate the potential capability of the bismuth oxide materials for use in extremely fast and low-voltage operation nonvolatile memories.

2.7 CONCLUSION

Elements of ferroelectric memory device technologies and their operating principles were overviewed with an emphasis on specification requirements of DRAMs and nonvolatile

![Fig. 2.19 Typical hysteresis loops for SrBi$_{2}$Ta$_{2-x}$Nb$_{x}$O$_{9}$ (SBTN) capacitors.](image)
memories from engineering and industrial points of view. It was shown that proper materials choice can provide solutions to the achievement of required electrical properties; Ba$_{1-x}$Sr$_x$TiO$_3$ for high-density DRAMs and SrBi$_2$(Ta,Nb)$_2$O$_9$ for nonvolatile memories. It was also emphasized that intrinsic electrical properties of ferroelectric films can be maintained and controlled throughout adequate fabrication processes which include: a liquid source misted chemical deposition (LSMCD) technique for film deposition control, a reactive ion etching (RIE) method using chloride mixtures for effective capacitor profile control, and a TiN/Ti barrier technology for suppressing the formation of SiO$_2$ at the ferroelectric/Pt interface. Integrated Ba$_{0.7}$Sr$_{0.3}$TiO$_3$ capacitors demonstrated a low leakage current of $2 \times 10^{-8}$ A/cm$^2$ at 3.3 V, a wide frequency dispersion range of up to 2 GHz, and a TDDB life of better than 10 years. The introduction of SrBi$_2$Ta$_2$O$_9$ into ferroelectric capacitors with Pt electrodes has resulted in a fatigue-free operation in polarization reversal for up to $10^{12}$ cycles at 10 MHz and 200 kV/cm. All these techniques indicate an engineering reality of manufacturing high-density DRAMs using high-dielectric-constant materials and will give rise to a new generation of FeRAMs using ferroelectric materials with confident reliability operating at fast speeds and low voltages.
3 Current–Voltage Characteristics of $\text{Ba}_{0.7}\text{Sr}_{0.3}\text{TiO}_3$ Capacitors

3.1 INTRODUCTION

Ferroelectric materials, such as $\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$ (BST), $\text{PbTiO}_3$ (PTO), and $\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$ (PZT), have emerged as high-dielectric-constant capacitor materials for high-density integrated circuit (IC) applications, such as dynamic random access memory (DRAM) cell capacitors. When they are incorporated into ICs, leakage current in these capacitors is one of the most important parameters for estimating the capacitor charge retention. Although a variety of data for the electrical properties of ferroelectric films with preliminary metal-insulator-metal (MIM) test structures have been reported, there are very few data related to the electrical properties of fully processed integrated capacitors. One of the major reasons arises from the fact that the leakage current readily increases to an unacceptable level when the ferroelectric capacitors undergo the backend integration process after the formation of the capacitor. For instance, thermal treatments in forming gases needed to stabilize the underlying metal-oxide-semiconductor (MOS) transistors sometimes cause serious damage to the ferroelectric capacitors. Therefore, to obtain a confident understanding of electrical behaviors of integrated ferroelectric capacitors, it is necessary to characterize the electrical properties of fully processed ferroelectric capacitors obtained through a well-controlled backend process.

In this chapter, we study the current-voltage ($J-V$) characteristics of fully processed integrated $\text{Ba}_{0.7}\text{Sr}_{0.3}\text{TiO}_3$ capacitors to provide a digital/analog filtering IC with an embedded bypass capacitor connected in parallel with the external power supply. Using
the fully processed integrated capacitors we attempt to extract the possible current transport mechanisms from the temperature dependence of the \( J-V \) characteristics.

### 3.2 EXPERIMENTAL

Among various ferroelectric materials, BST is one of the appropriate choices for realizing a high-dielectric-constant integrated capacitor because its stoichiometry is chosen to maximize the dielectric constant at the phase transition boundary. In the present experiments, \( \text{Ba}_{0.7}\text{Sr}_{0.3}\text{TiO}_3 \) films were prepared by a metal-organic decomposition technique on Pt-deposited silicon wafers in which the digital/analog filtering ICs are implemented already.

A metal alkoxide solution including 6 wt\% BST was coated on a 300-nm-thick Pt electrode on a Si wafer to obtain an about 185-nm-thick crystallized BST film. After high-temperature annealing of the coated films in oxygen, a 150-nm-thick Pt electrode was deposited on the crystallized BST to form a MIM structure and a number of capacitors with each size of \( 200 \times 200 \ \mu \text{m}^2 \) were patterned using a plasma etcher. Subsequently, the capacitors were covered with an interlayer silicon dioxide film formed by chemical vapor deposition and then the interlayer film was etched in plasma to form contact openings for interconnections between the capacitors and underlying peripheral MOS transistor circuits. After metallization with sputtered aluminum, interconnect patterns were formed by wet chemical processing. After post-metallization annealing in forming gas, a silicon nitride film for passivation was deposited by plasma chemical vapor deposition and then bonding pad openings were formed by dry etching.

The \( J-V \) characteristics of the fully processed BST capacitors integrated in the MOS device were measured with an HP4145B semiconductor parameter analyzer at different temperatures in the range of 300 – 423 K. The capacitance-voltage \( (C-V) \) characteristics were measured with an HP4194A impedance/gain-phase analyzer to observe the dielectric response of the BST films to low frequency electric fields. Optical dielectric constants of the BST films were measured with a Nano-Spec model 4000 microspectrometer.
3.3 RESULTS AND DISCUSSIONS

3.3.1 Process-Induced Resistance Degradation

Figure 3.1 shows typical $J-V$ curves of a BST capacitor after the patterning of the MIM-structured capacitor and after completion of the integration process. The leakage current at an applied voltage of 3 V of the fully processed capacitor was increased from $10^{-8}$ to $10^{-6}$ A/cm$^2$ during backend processing after the capacitor patterning. This increase in leakage current is ascribed to a resistance degradation of the BST films due to damage occurring during the backend processing such as sputtering of metals, etching of contact holes, deposition of dielectrics or passivations, forming of underlying transistors, or

![Semilogarithmic plot of conduction current versus applied voltage for a typical integrated BST capacitor with a size of 200×200 μm$^2$ and thickness of 185 nm. The lower curve is for the capacitor after patterning. The upper curve is for the fully processed capacitor.](image.png)
annealing of wafers. Even with the increase in leakage current, the fully processed capacitor is of sufficient quality for use in MOS devices as a bypass capacitor because the leakage current level is much smaller than the stand-by current, typically on the order of milliamperes, of these devices. Therefore it will be informative to study the leakage current behaviors of the fully integrated BST capacitors in relation to the designing of ferroelectric devices and the integration processes. In the present experiments the fully integrated BST capacitors were electrically tested for the leakage current in the temperature range from 300 to 423 K.

3.3.2 Temperature Dependence of Leakage Current

Figure 3.2 shows $J$–$V$ characteristics of the fully processed integrated BST capacitors

![Image showing J-V characteristics at different temperatures](image)

**Fig. 3.2** $J$–$V$ characteristics measured at temperatures of 300, 373, and 423K for fully processed integrated BST capacitors.
at temperatures of 300, 373, and 423 K. Since any asymmetry in the $J-V$ behavior did not appear upon reversal of the polarity of applied voltage and we have obtained a symmetric bias voltage dependence of the dielectric constant, as shown in Fig. 3.3, it can be assumed that $J-V$ characteristic of the BST capacitors are symmetrical with regard to the polarity of the applied field during the measurements. We will therefore hereafter study the situation in which the top electrode is positively biased and consider bulk-controlled and symmetric-interface-controlled conduction mechanisms.\textsuperscript{61-63} In Fig. 3.2, the leakage current is increased by several orders of magnitude as the temperature is elevated. When

**Fig. 3.3** Dielectric constant of an integrated BST capacitor as a function of dc bias voltage measured by applying a high frequency voltage of $\pm 0.5$ V at 1 MHz.
Fig. 3.4  A log–log plot of the $J$–$V$ curves in Fig. 3.2, showing the ohmic region below 1 V and different conduction behaviors above 2 V.

the curves in Fig. 3.2 are figured out on a log$J$ vs. log$V$ plot, as shown in Fig. 3.4, the $J$–$V$ characteristics can be separated into two distinct regions according to the slope of the curves. At low voltages below 1 V (50 kV/cm) the curves are represented by straight lines within the measured temperature range and each curve has a slope of approximately 1; this voltage dependence indicates an ohmic behavior. The curve measured at room temperature (300 K) is followed by another straight line at high voltages ( $> 2$ V, 100 kV/cm ) with a different slope of greater than 2. As the temperature is elevated (373 and 423 K), the $J$–$V$ characteristics exhibit different behaviors from the straight line at room temperature due to the contribution of other conduction mechanisms to the total current.
3.3.3 Current Transport Mechanisms at High Voltages

The current transport in ferroelectric films at high voltages is usually ascribed to the Frenkel-Poole and/or Schottky emission mechanisms,\(^{58,61-66}\) formulated as

\[
J = BV \exp \left[ -\frac{q\left(\phi_B - \sqrt{qV/\pi\varepsilon_0d}\right)}{kT} \right] \tag{3.1}
\]

and

\[
J = A'T^2 \exp \left[ -\frac{q\left(\phi_B - \sqrt{qV/4\pi\varepsilon_0d}\right)}{kT} \right], \tag{3.2}
\]

![Fig. 3.5](image-url)  
**Fig. 3.5** A \(\log(J/V) - \sqrt{V}\) plot showing the Frenkel-Poole conduction relationships at high voltages.
respectively, where \( q \) is the electronic charge, \( \phi_B \) is the trap depth for the Frenkel-Poole mechanism and the barrier height for the Schottky mechanism, \( V \) is the applied voltage across the capacitor with the thickness \( d \), \( \varepsilon_0 \) is the permittivity in vacuum, \( \varepsilon \) is the optical dielectric constant for electronic displacement, \( k \) is the Boltzmann constant, \( T \) is the absolute temperature, and \( A' \) and \( B \) are constants. If the current transport at high voltages is governed by either one of these two mechanisms, the \( J-V \) characteristics at high voltages should have a linear dependence on the square root of applied voltage and the slope of a curve in the linear region should give the value of \( \varepsilon \) (see Appendix A).\(^{65,66}\) To reveal these two mechanisms more clearly, the curves in Fig. 3.2 are replotted in Fig. 3.5.

**Fig. 3.6** A \( \log(J/T^2)-\sqrt{V} \) plot showing the Schottky relationships at high voltages.
for the Frenkel-Poole mechanism and in Fig. 3.6 for the Schottky mechanism. The slope of the curves at high voltages for the Frenkel-Poole mechanism yields $\varepsilon = 6.8$, 7.7, and 7.3, while for the Schottky mechanism the slope yields $\varepsilon = 2.8$, 3.9, and 4.1 at temperatures of 300, 373, and 423 K, respectively.

The dielectric constant of the BST film on a Pt-coated substrate was determined from an optically measured refractive index $n$. Since $n = 2.0$ at 640 nm in wavelength and $\varepsilon = n^2$, the optical dielectric constant is then calculated to be 4.0. As summarized in Table 3.1, the optical value of $\varepsilon$ is closer to those estimated from the Schottky mechanism than to those estimated from the Frenkel-Poole mechanism. This coincidence of the dielectric constants in the optical region indicates that the mobility of the electrons traveling in the BST film at high voltages is so high, $0.1 - 10 \text{ cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$, that the contribution from ionic displacements to the dielectric response is eliminated (see Appendix B).

At high voltages and high temperatures, the linear region in Fig. 3.5 is wider than that in Fig. 3.6. In addition, the linear region in Fig. 3.5 is enlarged and the onset voltage of the linear region is lowered as the temperature is elevated. These results indicate that the

<table>
<thead>
<tr>
<th>Temperature (K)</th>
<th>Dielectric Constant $\varepsilon$</th>
<th>Dielectric Constant</th>
<th>Fitting at High Voltages</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>Optical at 640 nm</td>
<td>Schottky</td>
<td>Frenkel-Poole</td>
</tr>
<tr>
<td>300</td>
<td>4</td>
<td>2.8</td>
<td>6.8</td>
</tr>
<tr>
<td>373</td>
<td>3.9</td>
<td>7.7</td>
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<tr>
<td>423</td>
<td>4.1</td>
<td>7.3</td>
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contribution of Frenkel-Poole emission to the leakage current emerges as the temperature is elevated in the high voltage region. The electrical conduction in the integrated BST capacitor at high voltages is therefore substantially dominated by the symmetrical Schottky interfaces within the measured temperature region and the bulk-controlled Frenkel-Poole emission begins to contribute to the total current at high temperatures.

3.3.4 Activation Energy

Figure 3.7 shows the activation energy plots of the current in the integrated BST capacitors at various applied voltages from 1 to 10 V. The current density increases by as
much as three orders of magnitude within the measured temperature range. The activation energy, plotted in Fig. 3.8, decreases with the square root of applied voltage and shows good linearity at high voltages. The linear dependence in the high voltage region is consistent with either conduction mechanism; Frenkel-Poole or Schottky emission. An extrapolation of the curve at high voltages gives a barrier height of 0.8 eV.

3.4 CONCLUSION

Leakage current behavior of fully processed BST capacitors implemented on a MOS device under various temperature and voltage conditions was investigated. The leakage
The current measured at 3V was increased from a value of $10^{-8}$ A/cm$^2$ when the capacitor was patterned to a value of $10^{-6}$ A/cm$^2$ when the integration process was completed. This increase in leakage current is assumed to be caused by a resistance degradation of the BST film due to damage occurring during integration processing. The leakage current of the fully processed capacitors, however, is small enough to be used in practical MOS devices as a bypass capacitor. For further understanding of integrated ferroelectric capacitors, we studied the temperature dependence of $J-V$ characteristics of the fully processed integrated BST capacitors. The current transport at low voltages ($<1$ V) is attributed to the ohmic conduction. At high voltages ($>10$ V), the Schottky mechanism is assumed to predominate, while the Frenkel-Poole mechanism begins to contribute to the leakage current as the temperature is elevated. The activation energy for the leakage current at high voltages was determined to be 0.8 eV.
Leakage Current Behavior of $\text{Ba}_{0.7}\text{Sr}_{0.3}\text{TiO}_3$ Capacitors during Stressing

4.1 INTRODUCTION

Because of the extensive evolution in integration technology of high-dielectric-constant ferroelectric materials such as $\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$ (BST), $\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$ (PZT), and $\text{SrBi}_2\text{Ta}_2\text{O}_9$ (SBT), integration of ferroelectric capacitors has been regarded as the most advanced technology to minimize and simplify the device structure of dynamic random access memories (DRAMs) beyond gigabit scales, as well as to realize nonvolatile ferroelectric memories. For practical memory applications of these materials, their electrical properties must be properly understood and kept stable for a period of operating time comparable with the minimum life of peripheral incorporated silicon devices. Among several reliability limiting factors originating from the ferroelectric capacitors in memory applications, degradation of the insulation resistance is the most crucial issue because it causes a change in stored charge in the ferroelectric capacitors for a certain period of the refresh cycle due to an increase in leakage current during long-term memory operation. Therefore the minimization of the variation in leakage current is a fundamental issue for memory applications of these ferroelectric materials.

A gradual increase in leakage current associated with the resistance degradation is commonly observed when temperature and dc voltage stresses are applied to ferroelectric capacitors for a certain period of time. Even under less excessive temperature and voltage stresses close to normal device operating conditions, much below the critical onset of instant breakdown, a slight increase in leakage current is still observed. Under excessive temperature and voltage stresses close to the occurrence of instant dielectric
breakdown, an anomalous increase in leakage current followed by eventual breakdown is observed. These degradation phenomena were modeled quantitatively based on the defect chemistry for multilayer ceramic capacitors. Similar phenomena have also been observed in BaTiO$_3$, BST, and PZT during the latter part of the life terminated by the eventual breakdown.

In this chapter, time-dependent leakage current behavior of integrated BST capacitors is studied. The sample capacitors used were separated into two types, each of which was obtained from different film growth process. The temperature dependence of current-voltage ($J-V$) characteristics of each type of capacitors is studied to reveal the predominant conduction mechanism under a given stress. The influence of the initial predominant conduction mechanism on the change in the $J-V$ characteristics during stressing is studied. A possible scenario, which describes the change in the conduction mechanism during stressing, is discussed.

4.2 EXPERIMENTAL

In the present experiments, Ba$_{0.7}$Sr$_{0.3}$TiO$_3$ films were prepared by metal-organic decomposition (MOD) using a homogeneous solution containing a stoichiometrically correct 6 wt% BST precursor. The MOD solution was spin-coated to form a BST film with a thickness of 185 nm on a 300-nm-thick Pt electrode on a Si wafer in which digital/analog filtering ICs are fabricated. The BST film was then annealed under a split condition at a high temperature in atmospheric oxygen, i.e., either at a rapid temperature ramp rate for sample A or at a slow temperature ramp rate for sample B. After the high temperature annealing, a Pt electrode with a thickness of 150 nm was deposited on the crystallized BST film to form a metal-ferroelectric-metal structure and a number of capacitors with each size of 200 $\times$ 200 $\mu$m$^2$ were patterned in a plasma etcher. Subsequently, the capacitors were covered with an interlayer silicon dioxide films formed by chemical vapor deposition and the interlayer film was etched in plasma to form contact openings to interconnect between the capacitors and underlying peripheral transistor
circuits. After the metallization with sputtered aluminum, interconnect patterns were formed by wet chemical processing. After post-metallization annealing in forming gas, SiN films were deposited for passivation and then bonding pad openings were formed by dry etching. Since the leakage current of ferroelectric capacitors without proper barriers is very sensitive to moisture, the SiN passivation is inevitable to ensure the reliability of all measurements in this experiment.

The \( J-V \) curves of the fully processed capacitors were measured on a hot stage with an HP4145B semiconductor parameter analyzer at different temperatures in the range of 300 – 423 K. Time-dependent leakage current behavior at elevated temperatures and high voltages was monitored with the same instruments. Long-term electrical degradation for up to 1500 h was evaluated by the leakage current measured at 3 V at room temperature before and after the integrated capacitors were subjected to high-temperature and high-voltage stresses.

### 4.3 RESULTS

#### 4.3.1 Initial \( J-V \) Characteristics

Since the film growth process influences the microstructure such as the grain size, grain boundaries, defect distribution, and interface states in the ferroelectric capacitors, it is anticipated that the \( J-V \) characteristics show different behaviors depending on the film growth conditions. Hence initial \( J-V \) measurements after the completion of integration processing were made to differentiate in the film quality between the type A and type B capacitors by considering interface-controlled and bulk-controlled conduction mechanisms.

First, the electrode interface-controlled current was studied. Figure 4.1 shows the \( J-V \) curves in a temperature range of 300 – 423 K for type A and type B capacitors after the completion of the integration process. The linear behavior of the curves at high voltages indicates the Schottky current and the slope yields the optical dielectric constant of the ferroelectric. Since both types of capacitors show the similar behavior at high voltages,
we can assume that the interface barrier height and the dielectric constant of type A capacitors are identical with those of type B capacitors.

Secondly, the bulk-controlled conduction in BST films was studied. In the presence of a large amount of defects in ferroelectric films, the leakage current at high temperatures at high voltages is frequently referred to as the Frenkel-Poole (F-P) conduction. Figure 4.2 shows log$J/V$ vs. $\sqrt{V}$ curves to reveal the linear $J-V$ behavior that follows the F-P conduction. Arrows in Fig. 4.2 indicate the points of approximate onset of the linear behavior on each curve. Unlike the curves in Fig. 4.2(b) for a type B capacitor, the curves in Fig. 4.2(a) for a type A capacitor show that the onset voltage of the linear behavior is lowered as the temperature is elevated. When the temperature is 423 K, for instance, the approximate onset voltage for the type A capacitor is 1.7 V while that for the type B capacitor is 7.0 V. At high temperatures, therefore, the leakage current of type A

Fig. 4.1 Initial $J-V$ curves on a log($J/T^2$) vs. $\sqrt{V}$ plot measured at 300, 373, and 423 K before stressing of (a) a type A capacitor annealed at a rapid ramp rate and of (b) type B capacitor annealed at a slow ramp rate.
Capacitors appears to be more strongly governed by the F-P mechanism even at low voltages than in type B capacitors. Since the F-P emission is due to field-enhanced thermal excitation of trapped carriers, we assume that type A capacitors are richer in Frenkel-type defects, both oxygen vacancies, metal vacancies, and interstitial metals, than type B capacitors.

![Initial J–V curves](image.png)

**Fig. 4.2** Initial $J$–$V$ curves on a log($J/V$) vs. $\sqrt{V}$ plot measured at 300, 373, and 423 K before stressing of (a) a type A capacitor annealed at a rapid ramp rate and of (b) type B capacitor annealed at a slow ramp rate. The onset voltage of the linear behavior of each curve is indicated by an arrow.

### 4.3.2 Time-Dependent Leakage Current Behavior during Stressing

Figure 4.3 shows time-dependent leakage current behaviors during stressing with 7 V at 473 K for $10^4$ s. At the beginning of stressing, both types of capacitors exhibited the same leakage current level. For the next hundred seconds, the leakage currents show
transient increases, instead of transient decrease in the ohmic region due to electrical charge hopping or dielectric polarization observed in PZT \cite{57,70} and BST,\cite{67} or due to charge absorption relaxation at distributed grain boundaries in SrTiO$_3$ and BaTiO$_3$,\cite{56} because the applied voltage, corresponding to a field of about 380 kV/cm, is much higher than the ohmic region below 50 kV/cm.\cite{56,66} After the transient regime the type A capacitor shows a further gradual increase in leakage current with time, whereas the type B capacitor exhibits a stable leakage current after a stress time of $10^3$ s. These time-dependent studies indicate that the leakage current under an excessive stress show different behaviors depending on the BST film growth conditions, even if the initial leakage currents are in the same level.

**Fig. 4.3** Time-dependent leakage current behavior of integrated BST capacitors during stressing at 7 V and 473 K. The upper curve is for a type A capacitor and the lower curve is for a type B capacitor.
4.3.3  $J$–$V$ Characteristics before and after Stressing

After being subjected to the high-temperature and high-voltage stress for $10^4$ s, $J$–$V$ characteristics of both types of capacitors were again measured at room temperature, as shown in Fig. 4.4. The leakage current of the type A capacitor increased by 4 orders of magnitude from the original level, whereas that of the type B capacitor increased by 2 orders of magnitude. When we assume the leakage current to be limited only by interface thermionic emission at the cathode, the leakage current at a given temperature is determined by the interface barrier height and the dielectric constant of the ferroelectric. Despite the increase in leakage current after stressing for both types of capacitors, the slopes at high voltages in terms of the dielectric constant are nearly identical to their original ones. This result implies that the increase in leakage current is due to the lowering of the interface barrier height rather than the change in the dielectric response. From the Schottky model described by Eq. (3.2), the lowering of the barrier height caused by the

![Fig. 4.4](image-url)

*Fig. 4.4*  $J$–$V$ curves on a $\log(J/T^2)$ vs. $\sqrt{V}$ plot for (a) a type A capacitor and (b) a type B capacitor measured at room temperature before and after stressing at 7 V and 473 K for $10^4$ s.
stress is calculated to be approximately 0.2 eV for the increase in leakage current of the type A capacitor and 0.1 eV for that of the type B capacitor.

4.3.4 Voltage Dependence of Long-Term Leakage Current Behavior

Long-term electrical degradation of the integrated capacitors was evaluated from the variation in leakage current at room temperature at 3 V after being subjected to a temperature of 423 K at different bias voltages, 3, 5, and 7 V, covering the possible operation voltage range expected from practical use conditions. The leakage current was measured at proper intervals during the entire stress duration for up to 1500 h. As shown in Fig. 4.5, the leakage current varies with stress time. However there is a definite difference

Figure 4.5: Variations in leakage current with stress time. The samples were subjected to stresses of positive applied voltages of 3, 5, and 7 V at 423 K for up to 1500 h. The leakage currents were measured at 3V at room temperature.
in the behavior of the leakage current between type A and type B capacitors. In type A capacitors, the leakage current ramps up in a short period of stress time for stress voltages from 3 to 5 V. Even for a stress voltage of 3 V, an anomalous increase in leakage current appears after 100 h. The leakage current in type B capacitors, on the other hand, increases slowly with time. For a stress voltage of 3 V, in particular, the leakage current is almost constant for up to 1500 h. The stress voltage of 3 V is much lower than the onset voltage (~7 V) of the F-P behavior in type B capacitors, while it exceeds the onset voltage (~1.7 V) of the F-P behavior in type A capacitors as seen in Fig. 4.2. When the stress voltage is increased to 5 or 7 V, which is higher than the onset voltages of the F-P emission in both types of capacitors, the leakage currents in type A capacitors increase faster than those in type B capacitors. These results indicate that the time-dependent increase in leakage current is significant when the leakage current under a given stress condition is dominated by the F-P mechanism.

4.4 DISCUSSION

4.4.1 Interface-Controlled Current

Since the F-P conduction is responsible for the time-dependent increase in leakage current, and the most likely traps for this mechanism are oxygen vacancies, we here postulate that the time-dependent change in leakage current is associated with the presence of oxygen vacancies. Many groups to date have pointed out the importance of the role of oxygen vacancies in the time evolution of the bulk-related leakage current of ferroelectric capacitors, i.e., a field-driven redistribution of oxygen vacancies in the films would result in formation of a forward-biased p-n junction. However, their arguments are limited in the change of the leakage current in the bulk. When the leakage current under consideration is originally predominated by the interface-controlled Schottky emission, we must take account of the change in leakage current at the interface as well as in the bulk. The difference between the present scenario and that discussed above is that the redistribution of oxygen vacancies now causes a change of the potential
barrier at the interface.

If the interface barrier height $\phi_B$ is achieved simply by the difference between the work function of the metal electrode $\phi_m$ and the electron affinity of the ferroelectric $\chi$, i.e.,

$$\phi_B = \phi_m - \chi, \quad (4.1)$$

a built-in potential $\phi_{bi}$ is formed across the depletion region within the ferroelectric near the interface (Fig. 4.6(a)). Then the total charge in the depletion region can consist of positively ionized oxygen vacancies and is attracted by the same amount of negative charge at the metal surface. When the temperature is elevated, the ionized oxygen vacancies initially distributed over the depletion region are thermally activated and may begin to migrate toward the cathode under a high electric field. After a long period of time, the ionized oxygen vacancies eventually accumulate near the cathode. The accumulated ionized oxygen vacancies give rise to the narrowing of the depletion region with increasing the electric field strength. As a result, a large built-in potential is established within a very narrow region in the vicinity of the interface. This condition allows electrons to tunnel through the potential barrier from the metal electrode into the ferroelectric under the high electric field. Then the tunnel emission will contribute to the total current as illustrated in Fig. 4.6(b). If the accumulation process proceeds much further, the situation will be similar to that of a metal-semiconductor contact with a high doping concentration. For a doped semiconductor, the energy difference between the conduction band edge $E_c$ and the Fermi level $E_F$ is given by

$$E_c - E_F = kT \ln \left( \frac{N_c}{N_D} \right), \quad (4.2)$$

where $k$ is the Boltzmann constant, $T$ is the absolute temperature, $N_c$ is the effective density of states in the conduction band, and $N_D$ is the donor density. Thus the higher the donor density, the lower the conduction band edge. Accordingly, further accumulation of ionized oxygen vacancies would result in the lowering of the potential barrier due to
degeneration of states near the cathode (Fig. 4.6(c)). Consequently, the contact resistance at the metal-ferroelectric interface is lowered effectively.

In either mechanism, the motion of oxygen vacancies is responsible for the increase in leakage current with time. Since the concentration of oxygen vacancies in type A capacitors is estimated to be greater than that in type B capacitors from the differences in the onset voltage of linear behaviors in Fig. 4.2 and from the voltage dependence of the long-term leakage current behaviors in Fig. 4.5, it is conceivable that the increase in leakage current in the presence of excessive temperature and voltage stresses is more likely to occur in type A capacitors than in type B capacitors.

![Figures 4.6](image)

**Fig. 4.6** Possible mechanisms for the lowering of the contact resistance at the metal-ferroelectric interface of a resistive BST capacitor across which a dc bias voltage is applied: (a) formation of the potential barrier, (b) accumulation of ionized oxygen vacancies to cause a large and narrow built-in potential, and (c) barrier lowering due to degeneration in the depletion region.
4.4.2 Bulk-Related Mechanisms

As a result of the lowering of the contact resistance at the cathode, the bulk-controlled conduction appears to be predominant. When the total leakage current reaches a certain threshold, a current limitation by the space charge comprised of the flowing current would take place, independent of whether the leakage current is bulk-controlled or interface-controlled (see Appendix C). The space-charge-limited current through a trap-free medium in steady state is well described by the trap-free square law. From the experimental result for a stress condition of 7 V and 423 K applied for $10^4$ s, both types of capacitors exhibited a decrease in the slope of the linear behavior toward a slope of 2 on log$_J$ vs. log$_V$ plots in Fig. 4.7. Since distributed oxygen vacancies are considered to be the dominant traps in the ferroelectric, the accumulation of the oxygen vacancies near the

![Fig. 4.7](image)

$J$–$V$ curves on a log$J$–log$V$ plot for (a) a type A capacitor and (b) a type B capacitor measured at room temperature before and after stressing at 7 V and 473 K for $10^4$ s.
interfaces may result in a lack of traps across the bulk of the ferroelectric. This argument is supported by the speculation that the contribution of the space-charge-limited current with the trap-free square law becomes predominant after the lowering of the barrier height took place. Therefore it can be speculated that the increase in leakage current of the integrated BST capacitors is caused by a change in the conduction process from the interface-controlled Schottky type to the bulk-related space-charge-limited type due to the redistribution of oxygen vacancies across the film during stressing.

4.5 CONCLUSION

We have shown the \( J-V \) characteristics of integrated BST capacitors and their time-dependent behavior under excessive temperature and voltage stresses for up to 1500 h. The \( J-V \) behaviors indicated a strong dependence on the film growth conditions. After excessive stressing, \( J-V \) curves indicated a change in the built-in potential giving rise to the lowering of the contact resistance at the metal-ferroelectric interface followed by an asymptotic fit to the space-charge-limited process. From the difference in the onset voltage of the Frenkel-Poole behavior between two types of capacitors with different film growth processes, the presence of oxygen vacancies was concluded to be responsible for the change in leakage current with time. The increase in leakage current is attributed to the accumulation of oxygen vacancies at the cathode, and eventually the space-charge-limited current becomes predominant.
5.1 INTRODUCTION

Nonvolatile ferroelectric memories using SrBi$_2$Ta$_2$O$_9$ (SBT), a material with a bismuth-layered perovskite structure, have stimulated much interest due to their extremely low polarization fatigue, a phenomenon that is induced by repetitive polarization switching. In addition, polarization in bismuth-layered perovskite thin film capacitors can be switched and saturated in a voltage range below 3 V, while ferroelectric thin film capacitors fabricated from materials with high remanent polarization, such as Pb(Zr,Ti)O$_3$ (PZT) or (Pb,La)(Zr,Ti)O$_3$ (PLZT), require high poling voltages of typically 5 V. For the use of bismuth-layered perovskite thin film capacitors in nonvolatile memory applications, charge retention, which is typically required to be longer than 10 years under specified temperature stresses, still remains as a fundamental reliability concern. It is therefore of interest to study the thermal stability of remanent polarization in ferroelectric memory capacitors fabricated from bismuth-layered perovskites. In this chapter, we investigate the charge retention characteristics of integrated SrBi$_2$(Ta,Nb)$_2$O$_9$ (SBTN) capacitors poled at 3 V. The test capacitors were integrated into a memory test structure on a silicon substrate with metal-oxide semiconductor (MOS) transistor circuitry operating at 3 V. The effects of storage temperature on remanent polarization are studied by measuring the switched and non-switched polarizations after high temperature baking in the temperature range from 27 to 150°C for selected periods of time.
5.2 EXPERIMENTAL

5.2.1 Sample Preparation

The SBTN films were prepared by metal-organic decomposition processing on Pt-deposited silicon wafers with integrated MOS circuitry for driving ferroelectric memories. Film thickness after annealing at high temperature in atmospheric oxygen was 240 nm. Following deposition of the top Pt electrode, capacitor arrays containing 110 elements each were patterned. The top electrode size of each capacitor element was $5 \times 5 \mu m^2$. Then the interlayer dielectric deposition, metallization, and passivation processes necessary for ferroelectric memory fabrication were carried out. Finally, the test capacitor arrays were assembled in ceramic packages with wiring.

5.2.2 Experimental Procedure

Figure 5.1 shows typical polarization vs. voltage ($P-V$) loops of an SBTN capacitor that has been allowed to relax for about 5 s after poling, where $P_s$ is the switched polarization for a capacitor in the up state, and $P_{ns}$ is the non-switched polarization for a capacitor in the down state both when a negative voltage pulse is applied (see Appendix D). In a ferroelectric memory cell with two transistors and two capacitors (2T/2C), a voltage difference on a bit-line pair corresponding to the acquired charges, $P_s$ and $P_{ns}$, is amplified for logic state discrimination. In the one-transistor and one-capacitor (1T/1C) cell architecture, the bit-line voltage in terms of either $P_s$ or $P_{ns}$ is also compared with a reference voltage. The hysteresis loop, therefore, should have a certain difference between $P_s$ and $P_{ns}$, defined as $P_{nv} = P_s - P_{ns}$, to generate a signal available to the sense amplifier. In either memory cell configuration, $P_{nv}$ must be greater than an incoming noise margin of the sense amplifier.

For the transient polarization decay measurement, the change in the voltage across the sense capacitor was monitored. Since there was a limitation in duration of the transient polarization measurement, a pulse polarization measurement technique was used for the retention test exceeding 530 ms. The pulse sequence used is shown in Fig. 5.2. The
Fig. 5.1  A typical hysteresis loop, showing charge losses after the storage for a certain period of time. (a) $P_s$: Switched polarization charge extracted from a capacitor in the up state. (b) $P_{ns}$: Non-switched polarization charge extracted from a capacitor in the down state.

Voltage pulses are triangular waves of $\pm 3$ V with a duration of 11 ms. The switched and non-switched polarizations, $P_s$ and $P_{ns}$, were measured as following steps: (1) Define the polarization state of a capacitor array with a cycle of negative and positive voltage pulses; (2) pole the capacitor array into the up state with a positive voltage pulse or the down state with a negative voltage pulse; (3) wait a few seconds at 27°C for the initial polarization measurement; (4) read $P_s$ from the capacitor in the up state and $P_{ns}$ from the capacitor in the down state, both with a negative voltage pulse at 27°C; (5) repeat step 2 for rewrite; (6) bake at selected temperatures (27, 75, 125, and 150°C) for the appropriate retention time; and (7) repeat step 4 for retention measurements. The $P-V$ measurements were performed using a Radiant Technologies RT6000SI tester. Each capacitor array was tested only once in order to prevent history-dependent effects such as imprint.
Fig. 5.2  Pulse trains used for the retention measurement. Prior to the test, a positive voltage pulse sets the polarization state of a capacitor into (a) the up state and a negative voltage pulse sets it into (b) the down state. The amount of retained polarization after baking is determined by applying a negative voltage pulse to the both states.

5.3  RESULTS

5.3.1  Time Dependence of Polarization Decay

Figure 5.3 shows $P_{nv}$ vs. retention time. The data set for the first 530 ms after poling was obtained from transient polarization measurements. The initial pulse polarization measurement was made at 10 s and the values of $P_{nv}$ at 27°C were approximately 12 $\mu$C/cm$^2$. After the initial pulse polarization measurement, test capacitors were baked at selected temperatures (27, 75, 125, and 150°C) for 2, 24, and 100 h. Values of $P_{nv}$ after storages at 27°C showed good agreement with a straight fitting line extrapolated from data points in the transient regime. It is therefore reasonable to extend the fitting line to 100 h, and is assumed that the decay in $P_{nv}$ is governed by a single mechanism in the short to
long time regime ($10^{-3}$ to $10^{5}$ s). The linear dependence of the decay curve on logarithmic time yields a decay rate of $0.24 \ \mu\text{C/cm}^2$ per decade at $27^\circ\text{C}$. The logarithmic time dependence suggests that the polarization decay process is associated with a wide distribution over orders of magnitude in relaxation time, and is described by$^{51,79-81}$

$$P(t) = P_0 - m \log\left(\frac{t}{t_0}\right),$$  \hspace{1cm} (5.1)

where $t$ is the time, $t_0$ is the specific time at which the linear behavior of $P(t)$ begins with respect to $\log t$, $P_0$ is the polarization at $t = t_0$, and $m$ is the decay rate.

Fig. 5.3 Charge retention characteristics of SBTN capacitors integrated in a nonvolatile memory test structure for baking temperatures of 27, 75, 125, and 150$^\circ\text{C}$ as functions of time, showing the change in nonvolatile component, $P_{\text{nv}} = P_s - P_{\text{ns}}$, where $P_s$ is the switched polarization and $P_{\text{ns}}$ is the non-switched polarization.
5.3.2 Temperature Dependence of Polarization Decay

At elevated storage temperatures, a 2-h storage resulted in a significant decrease in $P_{nv}$ by up to 4 $\mu$C/cm$^2$, depending on the storage temperature. However, measurements made at another 24- and 100-h storages showed no pronounced change in $P_{nv}$ within the measurement reproducibility. Thus the decrease in $P_{nv}$ at high temperatures is supposed to occur within a short time when the temperature is elevated, as seen in SBT.$^{82}$ To evaluate the temperature effect on $P_{nv}$, poled capacitors were baked at different temperatures from 27 to 220$^\circ$C only for 15 min whereas it is enough to give rise to such a decrease in $P_{nv}$. Supposing the second order transition near the Curie temperature, $T_c$, the values of $P_{nv}$ were plotted as a function of baking temperature, $T$, so as to obtain the relation between $P_{nv}$ and $(T_c - T)^{1/2}$. As shown in Fig. 5.4, an extrapolation from this data set represented by

![Fig. 5.4](image.png)

**Fig. 5.4**  Polarization charge difference $P_{nv}$ vs. baking temperature $T$, where $T_c$ is the Curie temperature. Polarization measurements were made at 27$^\circ$C after storing at temperatures from 27 to 220$^\circ$C for 15 minutes.
closed circles indicates a collapse of $P_{nv}$ at a temperature of 330ºC, which is close to an experimentally determined value of the Curie temperature for SBTN films.83)

To account for the temperature effect in the high temperature storage test, the long-time storage values of $P_{nv}$ in Fig. 5.3, whose measurements were made after 2- to 100-h storages, were overlaid on the same plot (Fig. 5.4). Then a good agreement in the temperature dependence between the long-time storage values and the 15-min storage values was obtained. This fact indicates that the decrease in $P_{nv}$ at high temperatures from its initial ($t_0 = 10$ s) value is primarily due to an instantaneous decrease in remanent polarization within 15 min and that the temperature dependence is quite similar to that of spontaneous polarization in the vicinity of the second order transition. The decrease in $P_{nv}$ caused at high temperatures is explained by the loss of measurable charge in the capacitor electrodes coupled with the polarization in accordance with the temperature dependence of polarization below $T_c$, which follows the second order transition. Therefore once the capacitors are stored at high temperatures, $P_{nv}$ is quenched to room temperature.

### 5.4 DISCUSSION

Small changes in $P_{nv}$ from 2- to 24- and 100-h storages at high temperatures lead to a supposition that $P_{nv}$ at high temperatures has a similar logarithmic time dependence to that at 27ºC. When discussing the origin of the distributed relaxation time for the decay in remanent polarization, one can indicates two possible factors: (1) a variation in coercive energy responsible for polarization reversal; and (2) a variation in the energy depth of charge traps responsible for space charge emission. When the first mechanism is invoked, the polarization decay process is governed by the stochastic switching of thermally fluctuating displacement dipoles from one well to the other in the double-minimum potential with distributed coercive potential barrier height. The second mechanism accounts for the decay in remanent polarization resulting from screening by space charges redistributed after poling. The decay rate is then determined by the internal electric field strength and also the amount of mobile space charges in the capacitor.
Fig. 5.5  Typical $P$–$V$ hysteresis curves for positively poled SBTN capacitors before (●) and after (○) storage at 125°C for 100 h, obtained by pulsed polarization measurements.

Although either process leads to the distributed relaxation time, there is a substantial difference between them. The thermal fluctuation process is reversible if the coercive energy distribution does not change with time. In contrast, the space charge redistribution process is irreversible, and as a result the final polarization state is more stable than the other. In ferroelectric materials, such memory effects are referred to as imprint, which can be described as the establishment of a preference in the poled direction. 84-86) This phenomenon was also observed in the SBTN samples used in this experiment. As shown
in Fig. 5.5, for instance, there is a definite deviation in the hysteresis loop before and after storage at 125°C for 120 h. Once imprint has occurred, the initial hysteresis loop is no longer restored even by polarization switching. This fact strongly indicates that the polarization decay process is accompanied by imprint caused by the space charge redistribution. This conclusion is consistent with a speculation that the decrease in polarization of SBT capacitors is independent of the reversal of domains.\textsuperscript{87} The time required for emitting trapped charges into the conduction band may depend on the variation in trap depth in energy, resulting in a logarithmic time dependence of the change in remanent polarization. In addition, the distribution of the trap depths responsible for transport of emitted charges is probably limited in a shallow range from the conduction band because the dominant traps are metal cations such as Bi\textsuperscript{3+} ions for holes and Ta\textsuperscript{5+} ions for electrons.\textsuperscript{88} It is therefore expected that the polarization decay rate exhibits a weak temperature dependence.

5.5 CONCLUSION

The temperature dependence of charge retention characteristics of integrated SBTN capacitors was studied. The primary decrease in remanent polarization during high temperature storing was attributed to an instantaneous decrease in remanent polarization in accordance with the behavior of spontaneous polarization in the vicinity of the second order transition temperature, while a small variation in remanent polarization is observed for additional storage times. The remanent polarization decay at 27°C showed good linearity to the logarithmic retention time over a wide range of $10^{-3} \rightarrow 10^5$ s. The logarithmic time dependence of the decay in remanent polarization was attributed to the distribution in energy depth of charge traps. Charges emitted from these traps are responsible for the irreversible change in resultant hysteresis loops.
6.1 INTRODUCTION

Ferroelectric memory devices based on bismuth-layered perovskites such as SrBi$_2$Ta$_2$O$_9$ (SBT) and SrBi$_2$(Ta,Nb)$_2$O$_9$ (SBTN) have become an important class of nonvolatile ferroelectric memories because of their fatigue-free nature, exceeding $1 \times 10^{12}$ read/write cycles. These ferroelectric memories must preserve the stored data without power supply for more than 10 years over a wide range of temperatures, from −10 to 70°C for consumer applications and between −40 and 85°C for industrial applications.

The nonvolatility in ferroelectric memories is achieved essentially by preserving a sufficient amount of charge, which couples with the remanent polarization, in a storage capacitor to yield a voltage signal on a bit-line greater than the marginal signal for a sense amplifier when a read voltage pulse is applied. However, the remanent polarization in ferroelectric capacitors using materials such as Pb(Zr,Ti)O$_3$ tends to decrease with not only increasing the temperature but also time. Therefore, the long-term stability of remanent polarization and the temperature effects on the data retention performance are of much interest in ferroelectric memory applications.

In this chapter, the temperature dependence of memory retention failures in an SBTN-based 288-bit ferroelectric memory device is studied. From statistical results of temperature-accelerated retention testing, possible failure mechanisms are discussed by introducing empirical reliability models that well explain the data retention characteristics of SBTN memories over a wide range of time.
6.2 EXPERIMENTAL

6.2.1 Sample Fabrication

For the present experiment, a 288-bit memory that incorporates SBTN cell capacitors was designed. The capacitor size is $5 \times 5 \, \mu m^2$. Each memory cell is comprised of two transistors and two capacitors (2T/2C) with a cell size of $182 \, \mu m^2$. The 288-bit memory is organized into 18 rows by 16 bits. A typical access time of the memory is 230 ns at 5 V and room temperature. The memory cell capacitors with Pt electrodes were fabricated using a spin-on technique on the silicon wafer with an underlying peripheral drive circuit. The memories were cut into dies, and assembled in ceramic package parts. Since destructive readout is essential for 2T/2C ferroelectric memory cells, each part was used only once in the retention test to eliminate past history effects such as imprint.

6.2.2 Memory Retention Test

Prior to storing test memory parts at high temperatures, a test data pattern was programmed (written) into each part at 2.43 V and 75°C. The programming voltage was chosen to be low enough, and the temperature was chosen to be the maximum for use in consumer applications. The programmed parts were then stored at temperatures of 125, 150, and 175°C for selected periods of retention time up to 2000 h. The baked parts were cooled to 75°C, and then their data integrity and functionality were tested at an operation voltage of 2.43 V. Any memory part with failing bits was rejected. For each test condition of temperature and retention time, 10 test parts were used.

6.3 RESULTS AND DISCUSSION

6.3.1 Polarization Decay Model

In Chapter 5, the linear dependence of the polarization decay curve on logarithmic time yields a decay rate of $0.24 \, \mu C/cm^2$ per decade at room temperature. The logarithmic time dependence suggests that the polarization decay process has a distribution over
orders of magnitude in relaxation time, and is described by \(^{51,79-81}\)

\[
P(t) = P_0 - m \log \left( \frac{t}{t_0} \right), \tag{6.1}
\]

where \(t\) is the retention time, \(t_0\) is the specific time at which the linear behavior of \(P(t)\) begins with respect to \(\log t\), \(P_0\) is the polarization at \(t = t_0\), and \(m\) is the decay rate (Fig. 6.1(a)).

### 6.3.2 Retention Failure Model

When the remanent polarization \(P(t)\) decays with time \(t\) at a constant decay rate of \(1/\tau\), the rate equation for the remanent polarization takes on the form

\[
\frac{dP(t)}{dt} = -\frac{1}{\tau} P(t), \tag{6.2}
\]

Then \(P(t)\) is not expressed as Eq. (6.1) but as

\[
P(t) = P_0^* \exp \left( -\frac{t}{\tau} \right), \tag{6.3}
\]

where \(P_0^* = P(0)\), and \(1/\tau\) is the rate constant for the decay. Let us assume that a memory device fails in a retention test when \(P(t)\) of a memory capacitor reaches a specific value, \(P_f\), which gives the lower limit of remanent polarization whose charge is detected by the sense amplifier, as illustrated in Fig. 6.1(b). Then we have an expression for the time to failure \(t_f\):

\[
t_f = \tau \log \left( \frac{P_0^*}{P_f} \right). \tag{6.4}
\]
In Eq. (6.3), $1/\tau$ can be regarded as the specific decay rate determined by the polarization decay mechanism. The temperature dependence of the rate constant is then expressed as

$$
\frac{1}{\tau} = \frac{1}{\tau_0} \exp \left( -\frac{E}{kT} \right),
$$

(6.5)

where $E$ is the specific activation energy, $k$ is the Boltzmann constant, $T$ is the absolute temperature, and $\tau = \tau_0$ at $E/kT = 0$. Combining Eqs. (6.4) and (6.5), we obtain the following relationship between temperature and time to failure:

$$
\log t_f = \frac{E}{kT} + \text{const.}
$$

(6.6)

![Diagram](image)

**Fig. 6.1** (a) A logarithmic decay model and (b) an exponential decay model for the remanent polarization applied to a sense circuit that can discriminate the logic states between “0” and “1” only when the remanent polarization is greater than a specific value of $P_f$. 

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This relationship is commonly referred to as the Arrhenius reaction model and is adequate as far as Eq. (6.3) is relevant to the decay process. However, the actual decay process is well described by Eq. (6.1). Let us assume again that a memory device fails when \( P(t) \) is equal to \( P_f \). From Eq. (6.1) this assumption leads to the following expression for time to failure:

\[
\log \left( \frac{t}{t_0} \right) = \frac{1}{m} (P_0 - P_f) \tag{6.7}
\]

If the slope \( m \) is regarded as the rate constant for the decay in remanent polarization given by Eq. (6.1), it has a form analogous to Eq. (6.5),

\[
m = m_0 \exp \left( -\frac{E}{kT} \right) \tag{6.8}
\]

where \( m = m_0 \) at \( E/kT = 0 \). From Eqs. (6.7) and (6.8), we obtain the following relationship between temperature and time to failure:

\[
\log \left[ \log \left( \frac{t_f}{t_0} \right) \right] = \frac{E}{kT} + \text{const.} \tag{6.9}
\]

Consequently, the temperature dependence of the time to failure in ferroelectric memories obeys the linear relationship between \( \log(\log t_i) \) and \( 1/T \).

### 6.3.3 Retention Failure Distribution

The distribution of times to failure obtained from the temperature-accelerated retention test on 288-bit memory parts was approximated to a log-normal distribution, as shown in Fig. 6.2. This approximation indicates that memory retention failures occur
when a threshold in remanent polarization $P_f$ is reached. In this figure, cumulative failures apparently increase as the baking temperature is elevated, and tend to saturate with time. The saturation of cumulative failures in the later part of retention time indicates a change in the failure mechanism and is a result of the lowering of the failure rate. Since the failure rate in the saturated regime appeared to be stabilized, a random failure mechanism characterized by a constant failure rate was adopted. Early failures during cumulative failures are rapidly increasing, on the other hand, were implicated in the relaxation process of remanent polarization described by Eq. (6.1), because the logarithmic time dependence leads to a significant change in $P_{av}$ in the earlier part of retention time. Therefore, the infant failure regime is characterized by a rapid increase in cumulative failure and the

Fig. 6.2 Lognormal plot of cumulative retention failures for 288-bit memory parts for a write voltage of 2.43 V.
failure distribution is approximated by fitting a straight line to a data set of cumulative failures that are increasing rapidly.

Figure 6.3 shows the temperature dependence of the time to 50% cumulative failure in the infant failure regime. The best fit of the temperature dependence given by Eq. (6.9) is obtained when the activation energy is 0.35 eV. Good linearity of the data in Fig. 6.3 supports the approximation that the decay in remanent polarization during the infant failure regime is governed by the logarithmic polarization decay process.

Since we assumed that the reliability of ferroelectric memories in the saturated regime is characterized by a random failure mechanism, the temperature dependence given by Eq. (6.6) was applied to the data set in this regime. In order to describe the failure times resulting from a random failure mechanism with a constant failure rate, the mean time between failures (MTBF) was calculated using the \( \chi^2 \) distribution for a 60% confidence limit (see Appendix E). The data used are the number of failing parts in the period of random failures with respect to the tested sample size for selected test durations at elevated temperatures, where infant failures are not included in the failure rate calculation. Figure 6.4 shows the temperature dependence of the MTBF. The fitting of the random failure model gives a straight line with an activation energy of 1.15 eV. This relationship can be used to predict the random failure rate at temperatures in the range of users’ application environment by extrapolating the fitting line.

6.3.4 Retention Failure Mechanism

As demonstrated in the experimentally fabricated ferroelectric memories, there are two different mechanisms for memory retention failures. Using Eq.(6.9), the activation energy associated with infant failures was calculated to be 0.35 eV. Once cumulative failures saturate, the memory retention failure is dominated by a random failure mechanism with an activation energy of 1.15 eV. The following argument deals with possible physical origins of these different failure mechanisms.

Let us first consider the infant failure mechanism, which follows the logarithmic time dependence of the polarization decay given by Eq. (6.1). There are two possible origins of
the logarithmic time dependence: (1) a variation in coercive energy responsible for polarization reversal; and (2) a variation in the energy depth of charge traps responsible for space charge emission. In the former, the reversal of thermally fluctuating dipoles from one well to the other in the double-minimum potential with distributed coercive potential barrier height is responsible for the decay in remanent polarization. This process is stochastic and continues until thermal equilibrium is established. In the latter, thermionic
Fig. 6.4 Failure time (MTBF) vs. temperature to show a random failure mechanism with an activation energy of 1.15 eV. The MTBFs were calculated using the $\chi^2$ distribution with a 60% confidence level.

The emission of trapped charges enhanced by the internal electric field promotes redistribution of space charges during the decay process. This process ends up when the total energy is minimized. As a result of the redistribution, the polarization charge is effectively screened by space charges such as electrons and holes emitted from the charge traps.

Although either process can cause a change in remanent polarization with time, there
is an obvious difference between them. The thermal fluctuation process is reversible because the coercive energy distribution does not change with time. In contrast, the space charge redistribution process is irreversible, so that the final polarization state is memorized temporally. In ferroelectric materials, such memory effects are referred to as imprint,\textsuperscript{84-86} which can be described as the establishment of a preference in polarization direction. As a result of imprint after storage at high temperatures, the hysteresis loop is no longer restored to the initial state. This distortion in the hysteresis loop is also observed in the SBTN capacitors used in this experiment, as shown in Fig. 5.7, and strongly implies that the polarization decay process is accompanied by imprint as a result of space charge redistribution. Another indication supporting the redistribution mechanism is the relatively small value of activation energy for infant failures obtained by applying the model following Eq. (6.9). Robertson\textit{ et al.} suggested a similar value for the depth of electron and hole traps in bismuth-layered perovskites.\textsuperscript{88} These shallow traps emit electrons and holes readily. It is therefore concluded that the infant failure of the SBTN ferroelectric memory is caused by the redistribution of space charges emitted from shallow traps. The time required for the space charge redistribution may depend on the defect density and stoichiometric deficiency in the film as well as storage temperature. It is therefore believed that there could be a distribution of trap depth, resulting in the logarithmic time dependence of the change in remanent polarization.

The random failure mechanism, in contrast, is characterized by a relatively high activation energy of 1.15 eV. In addition, microscopic failure analysis showed no distinct defects in failing capacitor elements. Since the activation energy obtained is close to that for the motion of oxygen vacancies and/or ionic impurities in the ferroelectric,\textsuperscript{86} the loss of polarization in failing capacitor elements is probably caused by the compensation or screening of the displacement dipole charges with mobile charges moving slowly at a certain rate determined by the activation energy. The memory retention failure rate in the random failure regime is therefore a function of the reaction rate of the mobile charges with displacement dipole charges and their concentration such as oxygen deficiency.
6.4 CONCLUSION

The temperature dependence of infant failures in a 288-bit SrBi$_2$(Ta,Nb)$_2$O$_9$ memory was fit to an empirical reliability model having a linear relationship between log(log($t_f$)) and $1/T$. Since this approximation yielded an activation energy of 0.35 eV similar to that of electron and hole traps in bismuth-layered perovskites and the process is irreversible, it is believed that infant failures are associated with the redistribution of electrons and holes in shallow traps. Random failures, on the other hand, exhibited a low failure rate with an activation energy of 1.15 eV similar to that for oxygen vacancies and/or ionic impurities.
Thermal Aging Effect in Poled Ferroelectric SrBi$_2$(Ta,Nb)$_2$O$_9$ Capacitors

7.1 INTRODUCTION

In nonvolatile ferroelectric memories, the number of write/read cycles without polarization fatigue (the endurance) and the data integrity without power supply are the most critical reliability concerns. In recent years, bismuth-layered ferroelectrics, such as SrBi$_2$Ta$_2$O$_9$ (SBT) and SrBi$_2$(Ta,Nb)$_2$O$_9$ (SBTN), have demonstrated excellent endurance performance by exceeding $10^{12}$ cycles. In contrast, temperature effects on the data integrity remain as a nonvolatile-memory-specific issue. When assessing the reliability performances related to the data integrity of ferroelectric memories, one should consider the following two aging effects observed during a given retention period: (1) relaxation and (2) imprint. Relaxation is characterized by the decay in retained polarization over a long period of time. Imprint, on the other hand, is characterized by the loss of switchable polarization from a preliminarily poled remanent state to the opposite (complementary) remanent state, resulting from the establishment of a preference for the preliminarily poled remanent state over the opposite remanent state during storage or unipolar voltage pulsing. Once imprint has occurred, a voltage offset appears in the polarization-voltage ($P-V$) hysteresis curve with increasing the coercive voltage from the preliminarily poled remanent state to the opposite remanent state. As a result, the remanent polarization of the opposite remanent state is decreased. Thus, imprint is implicated in the loss of switchable polarization from a preliminarily poled remanent state and is ascribed to the pinning of domains by charge carriers at
pinning centers. Early studies on BaTiO$_3$ and Pb(Zr,Ti)O$_3$ (PZT) bulks have explained the origin of the asymmetry in the $P-V$ hysteresis curve by the space charge effect. Similar reasoning has been adopted in the internal field development in PZT and (Pb,La)(Zr,Ti)O$_3$ (PLZT) thin films in terms of asymmetric distributions of electrons and oxygen vacancies. Although these aging processes have been described using empirical expressions, the origin of the time evolution and the temperature dependence of the decay in switchable polarization have not been explored.

In this chapter, we will examine thermal effects on the switchable polarization of SBTN capacitors. In order to determine the type of charge carrier in SBTN, the bias voltage dependence of the leakage current in SBTN capacitors is studied. With an assumption of carrier emission from traps distributed in the energy bandgap, an analytical model that accounts for the temperature effect on imprint in ferroelectric capacitors is introduced. Based on this model, the activation energy responsible for imprint in SBTN capacitors is inferred from the temperature dependence of the decay in switchable polarization that can be observed in deformed hysteresis curves.

7.2 EXPERIMENT

7.2.1 Sample Preparation

In the present experiments, 240-nm-thick SBTN capacitors were prepared by metal-organic decomposition processing on Pt-deposited silicon wafers with integrated metal-oxide-silicon devices for driving ferroelectric memories, followed by annealing at a high temperature in atmospheric oxygen. After deposition of the top Pt electrode on top of the ferroelectric layer, and subsequent patterning of 110 capacitor arrays with the top electrode size of $5 \times 5 \ \mu$m$^2$ each for accurate measurement of the polarization charge, the wafers with capacitors have experienced the interlayer dielectric deposition, metallization, and passivation processes necessary for ferroelectric memory fabrication. Finally, the test capacitor arrays were mounted in ceramic packages.
7.2.2  J–V Measurement

Current-voltage (J–V) characteristics of poled SBTN capacitors were observed before and after storage at high temperatures. Prior to J–V measurements, SBTN capacitors were positively poled to the top electrode with a voltage pulse of 3 V at room temperature. Then the J–V measurements on poled capacitors were made every 0.1 s after each 0.1 V applied voltage increment, from 0 to 5 V, and after each 0.1 V applied voltage decrement, from 0 to −5 V. After the initial J–V measurements, the test capacitors were again positively poled to the top electrode with a voltage pulse of 3 V at room temperature and subsequently stored at 125°C for 100 h. After high-temperature storage, J–V measurements were also made on the test capacitors in the same manner. An HP-4145B semiconductor parameter analyzer was used for the measurements.

7.2.3  Imprint Test Procedure

To examine the nonvolatility in hysteresis loops, pulse polarization measurements were made as part of retention testing. For instance, when a ferroelectric capacitor has been poled into one of the two possible states, and subsequently stored at an elevated temperature for a selected period of time, a voltage offset in the P–V hysteresis loop appears due to the preference for the up state over the down state. Imprint effects on the switchable polarization are then examined by measuring switched and nonswitched polarizations for the opposite state to the poled state for remanence, denoted by $P_s$ and $P_{ns}$, respectively, and the voltage offset in the P–V hysteresis loop. As in the two-transistor and two-capacitor (2T/2C) memory cell, a certain amount of difference between $P_s$ and $P_{ns}$, at least 1 μC/cm² typically, is required for discriminating the two logic states, logic “0” and logic “1”. We examined the imprint effect on the switchable polarization in terms of the polarization difference defined by

\[ P_{nv} = P_s - P_{ns} \]  

for the opposite state. Test sample packages, containing capacitors poled into known states,
were subjected to elevated temperatures of 75, 125, and 150°C for up to 100 h. Pulse polarization measurements were made at room temperature before and after high-temperature storage using triangular voltage pulses of ±3 V with a duration of 11 ms.

7.3 RESULT AND DISCUSSION

7.3.1 Imprint Effect on $J$–$V$ characteristics

Figure 7.1 shows typical $J$–$V$ curves for a positively poled SBTN capacitor before and after storage at 125°C for 100 h. The forward currents before and after high-temperature storage are identical. For the reverse currents, on the other hand, there appears a voltage shift of approximately 0.2 V between the anomalous current peaks due to polarization reversal. This voltage shift is a direct result of imprint and therefore agrees with the change in the coercive voltage in the $P$–$V$ curve, as shown in Fig. 5.5. At high reverse voltages ($< -2$ V), the reverse currents before and after high-temperature storage are also identical. These $J$–$V$ characteristics indicate that as a result of high-temperature storage there is no change in the spatial distribution of carriers leading to a change in the current transport in ferroelectric capacitors. However, SBTN capacitors exhibit definite imprint effects. This finding suggests that imprint is a localized effect in the ferroelectric capacitor. The asymmetry in the $J$–$V$ curves at high voltages ($> 2$ V and $<-2$ V) is strongly related to the type of majority carrier in the ferroelectric capacitor and is ascribed to the interfacial asymmetry when current transport is limited by electrode interfaces. The low forward currents at high forward voltages and high reverse currents at high reverse voltages indicate that electron injection is significant from the top electrode interface due to the interfacial irregularity associated with the surface roughness as a result of grain growth. Thus, it is believed that electrons are the majority carriers in the SBTN capacitors.
Fig. 7.1  Changes in the leakage current for a positively poled SrBi$_2$(Ta,Nb)$_2$O$_9$ capacitor before (●) and after (○) storage at 125°C for 100 h. The forward current measurement was followed by the reverse current measurement at room temperature.

7.3.2 Decay in Switchable Polarization

Here we consider a metal-ferroelectric-metal capacitor with an external bias source. When the ferroelectric capacitor is poled by applying a field, a remanent (spontaneous) polarization appears along the applied field in the ferroelectric capacitor even after the field is removed. If both metal electrodes are grounded after poling, the depolarization field due to polarization charges is equal to the opposed external field due to the compensating electrode charges, so that the macroscopic field in the ferroelectric capacitor
is zero at any time. Therefore, it appears that there are no macroscopic electric fields to cause a change in polarization of the ferroelectric capacitor. Nevertheless, ferroelectric capacitors exhibit an aging effect characterized by the decay in switchable polarization during high-temperature storage.\textsuperscript{85,102} This fact suggests that the imprint phenomenon is a manifestation of microscopic changes in the charge distribution of the ferroelectric capacitor.

Slow changes of the charge distribution which take a long time have been attributed to carrier emission into the conduction band from localized traps distributed in the insulating energy bandgap.\textsuperscript{105} For simplicity, we will consider the behavior of electrons for the negatively charged carriers. In the presence of charged traps in a ferroelectric, the situation may be illustrated by an energy band diagram, as shown in Fig. 7.2, in which most of the underlying traps below the Fermi level $E_F$ are occupied by electrons. In addition, some of the traps above $E_F$ are also occupied by thermally activated electrons. The distribution of charged traps per unit volume from the band edge to the bottom of the energy bandgap can be described by a possible distribution function $g(E)$, so that the number of traps lying in a narrow range of energy between $E$ and $E + dE$ per unit volume

\begin{figure}[h]
\centering
\includegraphics[width=0.8\textwidth]{fig72.png}
\caption{An energy band diagram in the presence of distributed charged traps in a ferroelectric. Grain boundaries are possible pinning centers with an}
\end{figure}
average potential barrier height of \( E_a \).

is given by \( g(E)dE \). Thus we have

\[
\int_0^\infty g(E)dE = N ,
\]  

(7.2)

where \( E \) is the energy depth from the bottom of the conduction band, \( g(E) \) is the distribution function of occupied traps per unit volume, and \( N \) is the total number of the occupied traps per unit volume. The number of electrons emitted into the conduction band from traps lying between \( E \) and \( E + dE \) during a short time interval between \( t \) and \( t + dt \) is proportional to the number of these traps, i.e.,

\[
r(t)dt = \alpha g(E)dE ,
\]  

(7.3)

where \( r(t) \) is the rate of electron emission into the conduction band from traps at an energy level of \( E \) per unit time and \( \alpha \) is the constant of proportionality. If the rate of electron emission from these traps into the conduction band is dependent on the energy depth, the waiting time \( t \) for the occurrence of electron emission from a trap at an energy depth of \( E \) is given by\(^{106}\)

\[
\frac{1}{t} = v_0 \exp\left( -\frac{E}{kT} \right) ,
\]  

(7.4)

where \( v_0 \) is the vibration frequency of trapped electrons, \( k \) is the Boltzmann constant, and \( T \) is the absolute temperature. From Eqs. (7.3) and (7.4), we have

\[
r(t) = \alpha kT g(E) \frac{1}{t} .
\]  

(7.5)

Then the rate of electron emission, \( R(t) \), from entire traps distributed in the energy
bandgap is given by

\[ R(t) = \int_0^\infty r(t) dE = \alpha NkT \frac{1}{t} \]  \hspace{1cm} (7.6)

It is immediately noticeable that \( R(t) \) is independent of \( g(E) \).

Here, we assume that domain pinning centers are distributed in the ferroelectric capacitor in a random manner and that the pinning centers capture encountered electrons at a constant rate. These pinning centers are preferably formed at grain boundaries or dislocation planes at which many electrons are trapped densely (Fig. 7.2). Therefore the band edge swells significantly in the vicinity of grain boundaries. In particular, the dense charged traps would give rise to potential barriers surrounding the pinning centers with an average barrier height of \( E_a \). Let we further assume that a certain fraction of switchable polarization is reduced by capturing an electron by a pinning center. Under this condition, the variation in \( P_{nv} \) with time follows

\[ \frac{dP_{nv}(t)}{dt} = -\beta R(t) P_{nv}(t) \]  \hspace{1cm} (7.7)

where \( \beta \) is a proportionality constant associated with electron capture. Substituting Eq. (7.6) into Eq. (7.7), we have the solution of Eq. (7.7) for a long period of time between \( t_0 \) and \( t \):

\[ P_{nv}(t) = P_0 \left( \frac{t}{t_0} \right)^{-m^*} \]  \hspace{1cm} (7.8)

where \( P_0 = P_{nv}(t_0) \) and

\[ m^* = \alpha \beta NkT \]  \hspace{1cm} (7.9)
This deduction can be confirmed by scattering the retention test data in a log $P_{nv}$ versus log$t$ plot, as shown in Fig. 7.3. The slope of the fitting line for a given storage temperature is equal to the value of exponent $m^*$ at the storage temperature under consideration. From the values of exponent $m^*$ at different temperatures, 75, 125, and 150°C, it turns out that the temperature dependence of $m^*$ is exponential rather than linear (Fig. 7.4). This consequence is congruent with an assumption that an electron approaching a pinning center must overcome the barrier height $E_a$ in order to be captured. Then, the coefficient $\alpha\beta$ in Eq. (7.9) is proportional to $\exp(-E_a/kT)$ because $\beta$ in Eq. (7.7) is related to the electron capture rate at the pinning center. Since the coefficient $kT$ in Eq. (7.9) does

![Figure 7.3](image_url)

**Fig. 7.3** $P_{nv}$ (= $P_s - P_{ns}$) of SrBi$_2$(Ta,Nb)$_2$O$_9$ capacitors switched into the opposite remanent state after high-temperature storage. $P_s$: Switched polarization acquired from a capacitor in the up state. $P_{ns}$: Nonswitched polarization acquired from a capacitor in the down state.
not vary appreciably with temperature relatively to the abrupt change in $\exp(-E_a/kT)$, we have

$$m^* = \gamma N \exp\left(-\frac{E_a}{kT}\right),$$  \hspace{1cm} (7.10)

where $\gamma$ is a constant. Although the expression for $P_{nv}$ in Eq. (7.8) is different form that in
Eq. (6.1), we shall see, in the following, that these two expressions are identical for \( t \gg 1 \) and \( m = m^* \ll 1 \).

By writing \( z = t/t_0 \), we can place \( 1 + z \) instead of \( z \) in Eqs. (6.1) and (7.8) for \( z \gg 1 \). When we expand \( \log(1 + z) \) in Eq. (6.1) into a Taylor series,

\[
P_{nv} = P_0 - m \left( z - \frac{z^2}{2} + \frac{z^3}{3} - \ldots \right).
\]  

(7.11)

On the other hand, when we expand \( (1 + z)^{-m^*} \) in Eq. (7.8) by using the binomial formula,

\[
P_{nv} = P_0 \left( 1 + z \right)^{-m^*}
\]

\[
= P_0 \left[ 1 - m^* z + \frac{m^* (m^* + 1)}{2} z^2 - \frac{m^* (m^* + 1) (m^* + 2)}{3} z^3 + \ldots \right].
\]  

(7.12)

For \( m^* \ll 1 \), the above equation is approximated as

\[
P_{nv} = P_0 \left[ 1 - m^* z + \frac{m^*}{2} z^2 - \frac{m^*}{3} z^3 + \ldots \right].
\]  

(7.13)

Putting \( m = m^* P_0 \), we have the same expression for Eqs. (6.1) and (7.8). In fact, Figure 7.4 indicates that the values of \( m^* \) are less than 0.1 for examined temperatures and the exponential temperature dependence yields \( E_a = 0.23 \) eV. Similarly, if Eq. (6.1) is applied to describe the behavior of \( P_{nv} \), \( m \) should have an exponential temperature dependence in the form

\[
m = P_0 \gamma N \exp \left( - \frac{E_a}{kT} \right).
\]  

(7.14)
From the values of $m$ obtained from $P_{nv}$ versus $\log t$ plots for different temperatures, $E_a$ is calculated be 0.19 eV, which is close to that obtained from $m^*$. As is anticipated from the argument on the distributed traps in the energy bandgap, the values are also close to those obtained from the temperature dependence of infant retention failure times for SBTN ferroelectric memories (0.35 eV). This coincidence in the value of activation energies leads us to believe that the decay in remanent polarization has the same origin that the decay in switchable polarization has. A possible explanation is that emitted electrons are captured by preferred pinning centers to screen or compensate the polarization charges as well as to pin the domains. Similar argument can also be made for holes as the positively charged carriers. The above argument leads us to a comprehensive understanding of imprint to be a result of the redistribution of emitted carriers, and also agrees with the deduction in the previous report that the relaxation in remanent polarization is due to the redistribution of carriers rather than polarization reversal. However, it should be noted that such redistribution of carriers must be highly localized because $J$–$V$ characteristics before and after high-temperature storage indicate that there is no macroscopic change in the entire charge distribution throughout the capacitor during the thermal aging process.

7.4 CONCLUSION

Current-voltage ($J$–$V$) characteristics of SrBi$_2$(Ta,Nb)$_2$O$_9$ capacitors before and after high-temperature storage indicated that carriers in SBTN are electrons and that imprint is a localized effect. An analytical model of the thermal aging process in poled ferroelectric thin film capacitors was introduced. The decay in switchable polarization with the power of time originates from the emission of electrons from traps distributed in the energy bandgap, while the exponential temperature dependence arises from the electron capture process associated with pinning centers. Based on this model, the temperature effect on the decay in switchable polarization was analyzed using high-temperature storage test data for SBTN capacitors. The temperature dependence of the decay in switchable polarization provided a thermal activation energy of 0.23 eV. Considering the role of thermally emitted...
electrons from traps, it was emphasized that the redistribution of electrons is responsible for both imprint and relaxation processes in SBTN capacitors.
Summary

With continuous advances in integration and ferroelectric materials technologies, integrated ferroelectric memories have emerged out as a reliable and cost effective alternative to traditional silicon memories with a commercial reality. In this thesis the author dealt with electrical degradation issues in integrated ferroelectric capacitors, which are potential reliability concerns for use in DRAMs and nonvolatile memories. To understand fundamental degradation mechanisms causing various failures in integrated ferroelectric memories, the author explored the motion of space charges in ferroelectric materials brought by ions such as ionized oxygen vacancies and electrons and holes emitted from traps. In particular, it was clarified that the motion of oxygen vacancies residing at deep levels (~ 1 eV) in the energy bandgap are responsible for the gradual increment in the leakage current in Ba_{1-x}Sr_xTiO_3 (BST) capacitors for DRAM applications, whereas redistribution of electrons and holes emitted from shallow traps (~ 0.2 eV) is a dominant aging process in poled SrBi_2(Ta,Nb)_2O_9 (SBTN) capacitors for nonvolatile memory applications. The following briefly summarizes the conclusions obtained throughout this work:

Chapter 2:
- Proper materials choice can provide solutions to the achievement of required electrical properties; BST for high density DRAMs and bismuth-layered ferroelectrics, such as SrBi_2Ta_2O_9 (SBT) and SBTN, for nonvolatile memories.
- Advanced ferroelectric integration techniques have been developed: A liquid source misted chemical deposition technique which provides conformal step coverage of
ferroelectric films, a reactive ion etching method using chloride mixtures enabling effective ferroelectric capacitor profile control, and a TiN/Ti barrier technology for suppressing the formation of a SiO₂ interlayer at the ferroelectric/Pt interface.

- A low leakage current of \(2 \times 10^{-8}\) A/cm² at 3.3 V, a wide frequency dispersion range of up to 2 GHz, and a TDDB life of better than 10 years have been achieved in integrated BST capacitors.

- The materials choice of SBT for ferroelectric capacitors with Pt electrodes has resulted in a fatigue-free operation in polarization for up to \(10^{12}\) voltage cycles at 10 MHz and 200 kV/cm.

Chapter 3:

- The temperature dependence of \(J-V\) characteristics of the fully processed integrated BST capacitors accounted for the leakage current behavior with the following mechanisms: (1) The current transport at low voltages (< 1 V) is ohmic. (2) At high voltages (> 10 V), the Schottky mechanism is predominant, while (3) the Frenkel-Poole mechanism begins to contribute to the leakage current as the temperature is elevated.

Chapter 4:

- From the difference in the onset of the Frenkel-Poole behavior between two types of capacitors obtained from different film growth processes, the presence of oxygen vacancies was concluded to be responsible for the change in leakage current with time.

- The increase in leakage current during stressing for a long period of time does not appear when the voltage stress is lower than the onset voltage of the Frenkel-Poole conduction.

- The increase in leakage current is caused by the lowering of the contact resistance at the metal-ferroelectric interface as a result of accumulation of oxygen vacancies, resulting in the emergence of the bulk-controlled current.
Chapter 5:
- The remanent polarization decay at 27°C showed good linearity to the logarithmic storage time over a wide range of $10^{-3} - 10^5$ s with a decay rate of 0.24 $\mu$C/cm$^2$ per decade in time.
- The primary decrease in remanent polarization during high temperature storing was attributed to an instantaneous decrease in remanent polarization in accordance with the behavior of spontaneous polarization in the vicinity of the second order transition temperature, while a small variation in remanent polarization is observed for additional storage times.
- The logarithmic time dependence of the decay in remanent polarization was attributed to the distribution in energy depth of charge traps.
- Charges emitted from the traps are responsible for the irreversible change in resultant hysteresis loops.

Chapter 6:
- The temperature dependence of infant retention failures in a 288-bit SBTN memory was fit to an empirical reliability model having a linear relationship between $\log(\log t_f)$ and $1/T$.
- Infant retention failures in the 288-bit SBTN memory are associated with redistribution of electrons and holes in shallow traps because the activation energy for the infant retention failures (~0.35 eV) is close to the depth of electron and hole traps in bismuth-layered perovskites and the process is irreversible.
- The random retention failures exhibited a low failure rate with an activation energy of 1.15 eV similar to that for oxygen vacancies and/or ionic impurities.

Chapter 7:
- Current-voltage ($J-V$) characteristics of SrBi$_2$(Ta,Nb)$_2$O$_9$ capacitors before and after high-temperature storage indicate that carriers in SBTN are electrons and associated with a localized pinning effect.
- The decay in switchable polarization originates from electron emission from
distributed traps in the energy bandgap, while the exponential temperature dependence arises from the electron capture process associated with pinning centers.

- An analytical model introduced implies that the thermal aging process in poled ferroelectric thin film capacitors follows the power of time.
- The temperature dependence of the decay in switchable polarization provided a thermal activation energy of 0.23 eV for capturing of electrons by pinning centers.

Throughout the work on electrical properties and degradations of ferroelectric capacitors, the author has reached the following two important conclusions:

1. Instabilities in $J-V$ characteristics of integrated ferroelectric BST capacitors originate from the field-driven motion of oxygen vacancies, which were induced by stoichiometric deficiency.

2. Local redistribution of charge carriers thermally emitted from traps is responsible for both relaxation of retained polarization and imprint in ferroelectric SBTN capacitors, whose thermal activation energies are characterized by the small values ranging from 0.2 to 0.4 eV. As far as random failures in substantial ferroelectric memories are concerned, however, oxygen vacancies become predominant for the polarization decay for long periods of time.

In this thesis, the author explained how the electrical degradations in integrated ferroelectric capacitors are intimately correlated with the motion of charge carriers by assuming acceptable kinetic models of charge carriers and defects. These models are fairly valid for considering and estimating the qualitative or long-term behavior of electrical characteristics of integrated ferroelectric capacitors. However, we have not reached any direct participants in such electrical degradation phenomena. In order to establish more confident and reliable electrical degradation models, we still need to identify the species of charge carriers exactly with more complementary sets of analytical data on the defect
densities and their energy levels. When these remaining issues are solved, we will be able to describe and control the behavior of electrical characteristics of integrated ferroelectric capacitors more definitely. Hence we need to address the instabilities and reliability issues in integrated ferroelectric capacitors discussed in this thesis through further improvements in process, device, and circuit designs to eliminate, minimize, or mitigate the ferroelectric degradation effects. Such approaches should be conducted properly according to envisaged applications and include: low-voltage operation memory circuitry, stacked memory cell integration, damage-less processing, and degradation-hard ferroelectric materials. Finally, the author hopes that the understandings of electrical degradation mechanisms in ferroelectric capacitors, obtained throughout this work, put forward the continued ferroelectric memory development effort and will evolve ferroelectric memories to be a major manufacturing segment of semiconductor industry in the 21st century.
ACKNOWLEDGMENTS

I am grateful to Prof. K. Matsushige of the Graduate School of Engineering, Kyoto University, for reviewing and commenting upon the manuscript and offering several important and valuable suggestions through the guidance. Prof. H. Matsunami of the Graduate School of Engineering, Kyoto University, reviewed the manuscript with great care and provided me with many constructive comments. I also thank Prof. H. Nozawa of the Graduate School of Energy Science, Kyoto University, for his kind tutelage and advice in the course of writing the manuscript. I wish to acknowledge valuable discussions with Profs. M. Suzuki and K. Tachibana of the Graduate School of Engineering, Kyoto University.

My thanks are extended to those who gave me an opportunity to delve into a diversity of integrated ferroelectric memories: Dr. D. Ueda, Director of the Semiconductor Devices Research Center, Semiconductor Company, Matsushita Electric Industrial Co., Ltd.; M. Kazumura, former Director of the Semiconductor Devices Research Center and current President of Toyo Dempa Co., Ltd.; T. Otsuki, General Manager of the IC Card Business Group, Semiconductor Company of Matsushita; Dr. S. Koike, President of Semiconductor Company of Matsushita; and Dr. G. Kano, Professor of the Graduate School of Kochi University of Technology. In particular, the writing of Chapter 2, covering the technical background and latest achievements in the field of ferroelectric memories, would not have been possible without the help and involvement of many colleagues in Matsushita. I would like to thank Dr. K. Inoue, Manager of the Semiconductor Devices Research Center, Semiconductor Company, Matsushita, for reading the entire manuscript. Thanks are also due to the staff of Symetrix Corporation, especially to Dr. C. A. Paz de Araujo, Chairman and Co-CEO, and L. D. McMillan, President and CEO, for technical cooperation and valuable discussions through the collaborative R&D program on ferroelectric memory materials and devices. Drs. Y. Watarai, K. Wani, and the late Y. Ogata were my first tutors at the Electronics Research Laboratory, Matsushita Electronics Corporation.

Finally, I owe a lasting debt of gratitude to my family for their indescribable support and encouragement without repayment.
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100. G. E. Pike, W. L. Warren, D. Dimos, B. A. Tuttle, R. Ramesh, J. Lee, V. G. Keramidas, and J. T.
A. Schottky and Frenkel-Poole Emissions

The electrostatic potential of an electron in the dielectric distant from the metal interface by \( x \) is derived from the mirror image field \( E \):

\[
E = \frac{q}{4\pi\varepsilon\varepsilon_0 (2x)^2},
\]

(A.1)

where \( q \) is the electron charge, \( \varepsilon \) is the dielectric constant of the dielectric, and \( \varepsilon_0 \) is the vacuum permittivity (Fig. A.1(a)). Then the electron emitted from the metal surface travels in an electrostatic potential \( \phi \), which is given by

\[
\phi(x) = -\frac{q}{16\pi\varepsilon\varepsilon_0 x}.
\]

(A.2)

In the presence of an applied field \( E_{ex} \), the effective potential is given by\(^{1,2}\)

\[
\phi(x) = -\frac{q}{16\pi\varepsilon\varepsilon_0 x} - E_{ex} x.
\]

(A.3)

The maximum potential appears at

\[
x_m = \frac{q}{\sqrt{16\pi\varepsilon\varepsilon_0 E_{ex}}},
\]

(A.4)

which yields a drop in \( \phi(x) \) from the vacuum level by

\[
\Delta \phi(x_m) = \frac{q}{16\pi\varepsilon\varepsilon_0 x_m} + E_{ex} x_m = \sqrt{\frac{q E_{ex}}{4\pi\varepsilon\varepsilon_0}}.
\]

(A.5)

---

This drop in $\phi(x)$ is the Schottky effect, which promotes the electron emission from the metal into the dielectric.

On the other hand, the electric field $E$ in the bulk at a distance $x$ from the center of a charged trap from which an electron is escaping is given by

$$E = \frac{q}{4\pi\varepsilon_0 x^2}. \quad (A.6)$$

In the presence of an applied field $E_{ex}$, the imprisonment potential of the electron in the charged trap is lowered by $^3$

---

**Fig. A.1** Formation of the electrostatic potential at which an electron is moving away (a) from a metal surface and (b) from a charge trap.

---

The lowering of the barrier height along the applied field enhances the hopping of the electron from the trap to the next, which mechanism is the origin of the Frenkel-Poole current in the dielectric.

From Eqs. (A.5) and (A.7), it turns out that the lowering of the potential barrier for the Frenkel-Poole mechanism is two times greater than that for the Schottky mechanism. This is the cause of the difference in the slope of the $J$ vs. $\sqrt{V}$ characteristics between the Frenkel-Poole current and the Schottky current.

\[ \Delta \phi(x_m) = \sqrt{\frac{qE_x}{\pi \varepsilon \varepsilon_0}}. \]  

\text{(A.7)}

**B. Dielectric Constant of Ferroelectrics**

There is a definite difference between the values of the dielectric constant at high frequency, evaluated from the refractive index in the optical region, $\varepsilon = n^2$, and those determined in static fields. The dielectric constant appears in the Schottky expression in Eq. (3.2) in Chapter 3 reflects the dielectric response of the dielectric to the fields diverging from emitted carriers, because the emitted carriers travel in the dielectric under the influence of polarization field as well as under the applied field. If the velocity of an emitted carrier is fast enough, the field diverging from the carrier also travels fast just like an impulse. Since the dielectric constants obtained from the Schottky current-voltage relationship are close to that obtained from an optical measurement ($\varepsilon = 4$), the dielectric response to the impulse field is almost in the optical frequency region, $\sim 10^{14}$ s$^{-1}$ at 640 nm in wavelength.

In such a high frequency region, only the bound electrons in the ionic cores can follow the change of the field. This leads us to make a rough estimation of the velocity of the emitted carriers from the dielectric response in the optical region. If the displacements of the bound electrons are on the order of less than 1 Å, the velocity of the bound electrons following the change of the field is calculated approximately to be $1 \, \text{Å} \times 10^{14} \, \text{s}^{-1} = 10^6$
cm·s\(^{-1}\), which should agree with the value of the velocity \(v_e\) of the emitted carriers. If the initial momentum of the emitted carriers is still conserved after emission, we can regard \(v_e\) as the drift velocity. Under the field \(E = 500\) kV/cm at which the Schottky current dominates, the mobility \(\mu\) of the carriers is calculated to be

\[
\mu = \frac{v_e}{E} \approx 1\ \text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}.
\]  

(A.8)

This value agrees with those reported for electrons or holes in perovskite-type titanates, \(0.1 - 10\ \text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}\).\(^4\) If BST is an \(n\)-type semiconductor, electrons are the majority carriers.

C. Space-Charge-Limited Current

The space-charge-limited (SCL) current in steady state is a current that flows in a dielectric capacitor under a limitation on the charge distribution of transporting carriers across the dielectric.\(^5\) This current limitation will take place, independent of whether the leakage current is bulk-controlled or interface-controlled, when the total leakage current reaches a certain threshold such as a punch-through condition for short-channel devices.\(^6\)

The total charge \(Q\) of carriers involved in the interior space of the dielectric is given by

\[
Q = CV,
\]  

(A.9)

where \(C\) is the capacitance per unit area and \(V\) is the voltage applied across the capacitor with a dielectric thickness of \(d\). Then the SCL current is given by

\[
J = \frac{Q}{\tau},
\]  

(A.10)

where \(\tau\) is the transit time of the charge \(Q\) across the dielectric. From


\[ C = \frac{\varepsilon \varepsilon_0}{d} \]  \hspace{1cm} (A.11)

and

\[ \tau = \frac{d}{\mu E} \]  \hspace{1cm} (A.12)

we have the trap-free square law for the SCL current:

\[ J = \frac{\varepsilon \varepsilon_0 \mu}{d^3} V^2. \]  \hspace{1cm} (A.13)

Using the static dielectric constant for the distributed charge independent of time, we can calculate the trap-free SCL current for the 185-nm thick BST capacitor as to be on the order of \( 100 V^2 \) A/cm\(^2\), which is much higher than those observed. However if the momentum of the emitted carriers is lowered due to the scattering or trapping (cf. Appendix B), the mobility of carriers can be lowered by orders of magnitude. Then the SCL current would be lowered to those observed in the BST capacitors (\( 10^{-4} \) - \( 10^{-1} \) A/cm\(^2\)) after being subjected to temperature and voltage stresses.


\[ 8 \text{ C. B. Sawyer and C. H. Tower, “Rochell salt as a dielectric,” Phys. Rev. 35, 269 (1930).} \]

D. Principle of Hysteresis Measurement

Hysteresis measurements on ferroelectric capacitors were made using a Sawyer-Tower circuit, which has received a historical consensus as a standard technique to characterize non-linear capacitors. Figure A.2(a) shows a typical circuit configuration. A ferroelectric capacitor of \( C_f \) and a sense capacitor of \( C_s \) are connected in series to a triangular ac voltage source, where \( C_f \) should be chosen to be much smaller than \( C_s \) so as to ignore the voltage drop across the sense capacitor. Since the voltage across the sense capacitor is given by \( Q/C_s \), where \( Q \) is the charge stored in each capacitor and obtained by
integrating the current flowed through the ferroelectric capacitor over a measurement cycle, a hysteresis curve is obtained as illustrated in Fig. A.2(b) by connecting the voltage source and sense capacitor to the X and Y inputs of an oscilloscope, respectively. Figure A.3 shows the signal responses from the sense capacitor in accordance with the applied voltage across the ferroelectric capacitor. Each turning point in the voltage cycle is numbered in order in accordance with the numbers on the hysteresis excursion in Fig. A.2(b). Since the voltage generator charges up the ferroelectric capacitor through an output impedance of $R_o$, the measurement speed is limited by the time constant. In addition, impedance matching should be considered for higher frequency measurements.$^9,^{10}$ Thus there is a limitation on the capacitance of ferroelectric capacitors measurable with such a system. In the present experiment, the transient measurement of the polarization decay after poling was made by monitoring the voltage across the sense capacitor. The limiting time for the transient measurement was 530 ms in our case.

---

Fig. A.2  (a) A Sawyer-Tower circuit for hysteresis measurements. (b) A typical hysteresis curve.

---


Fig. A.3 Waveforms of (a) the voltage applied across, (b) current flows through, and (c) charge stored in a ferroelectric capacitor during a hysteresis measurement cycle, where $V_p$ is the amplitude of the cycling voltage across the ferroelectric capacitor, $P_r$ is the remanent polarization and $P_{\text{sat}}$ is the saturation polarization.
E. Failure Rate Calculation

Both the infant mortality and random failure rate regions can be described through the same types of calculations. During this time the probability of failure density function \( f(t) \) is well expressed by the equation

\[
f(t) = \lambda e^{-\lambda t}
\]  

(A.14)

where \( \lambda \) is the failure rate and \( t \) is time. The failure rate \( \lambda \) represents the instantaneous rate of failure for units of a population that have survived to time \( t \). Since \( \lambda \) is changing rapidly during infant mortality, the expression does not become useful until the random failure period, where \( \lambda \) is relatively constant. Another measure of reliability is the mean time to failure (MTTF) or mean time between failures (MTBF), both being equal to the reciprocal of the failure rate, when \( \lambda \) is constant, having units of hours, and being given by

\[
\text{MTBF} = \bar{t} = \int_{0}^{\infty} tf(t) dt = \int_{0}^{\infty} t \lambda e^{-\lambda t} dt = \frac{1}{\lambda}.
\]  

(A.15)

According to the concepts of the central limit theorem, the values of any samples of units out of a large population will produce a normal distribution. Since reliability evaluations usually involve only samples of an entire population of devices, \( \lambda \) is calculated using the \( \chi^2 \) distribution from the equation:

\[
\text{MTBF} = \frac{1}{\lambda} = \frac{2n \tau}{\chi^2 (2(r+1), \alpha)}.
\]  

(A.16)

where

\[
\alpha = \frac{100 - \text{CL}}{100},
\]  

(A.17)

CL is the confidence limit in percent, \( n \) is the total number of tested devices, \( \tau \) is the duration of test, and \( r \) is the number of rejects. The confidence limit is the degree of
conservatism desired in calculation. A 50% confidence limit is the best estimate and is the mean of the expected values of $\lambda$. A 60% confidence limit is a little more conservative value and results in a higher $\lambda$ which represents the point at which 60% of the population of the values of $\lambda$ is considered. The term $2(r+1)$ is called the degree of freedom and is an expression of the number of rejects in a form suitable to $\chi^2$ tables.
PUBLICATIONS

[with related chapter number(s)]


